AON7262E

60V N-Channel AlphaSGT™

General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- ESD protected

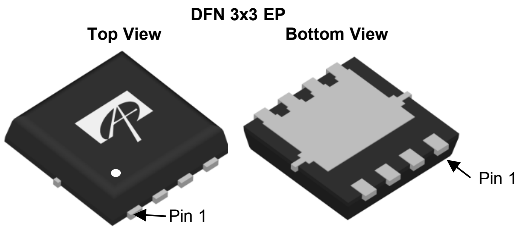
Applications

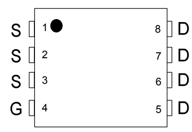
- High efficiency power supply
- Secondary synchronus rectifier

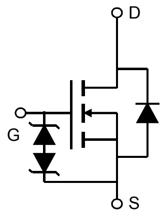
Product Summary

V_{DS}	60V
I_D (at V_{GS}=10V)	34A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 6.2mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 8.5mΩ
Typical ESD protection	**HBM Class 2**

100% UIS Tested
100% Rg Tested







Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON7262E	DFN 3x3 EP	Tape & Reel	5000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	34	A
	T_C=100°C		34	
Pulsed Drain Current [C]		I_{DM}	135	
Continuous Drain Current	T_A=25°C	I_{DSM}	21	A
	T_A=70°C		17	
Avalanche Current [C]		I_{AS}	23	A
Avalanche energy	L=0.3mH [C]	E_{AS}	79	mJ
V_{DS} Spike [I]	10µs	V_{SPIKE}	72	V
Power Dissipation [B]	T_C=25°C	P_D	43	W
	T_C=100°C		17	
Power Dissipation [A]	T_A=25°C	P_{DSM}	5.0	W
	T_A=70°C		3.2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	20	25	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		45	55	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	2.9	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA		1.2	1.65	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			4.8	6.2	mΩ
			T_J=125°C		7.8	10	
		V_{GS}=4.5V, I_D=18A			6.2	8.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			75		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			0.7	1	V
I_S	Maximum Body-Diode Continuous Current [G]					34	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz			1652		pF
C_{oss}	Output Capacitance				520		pF
C_{rss}	Reverse Transfer Capacitance				52		pF
R_g	Gate resistance	f=1MHz		0.6	1.3	2.0	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=20A			30	45	nC
Q_g(4.5V)	Total Gate Charge				15	25	nC
Q_{gs}	Gate Source Charge				3.5		nC
Q_{gd}	Gate Drain Charge				6.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=1.5Ω, R_{GEN}=3Ω			6		ns
t_r	Turn-On Rise Time				5		ns
$t_{D(off)}$	Turn-Off DelayTime				29		ns
t_f	Turn-Off Fall Time				7		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs			19		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs			60		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
I. The spike duty cycle 5% max, limited by junction temperature TJ(MAX)=125° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

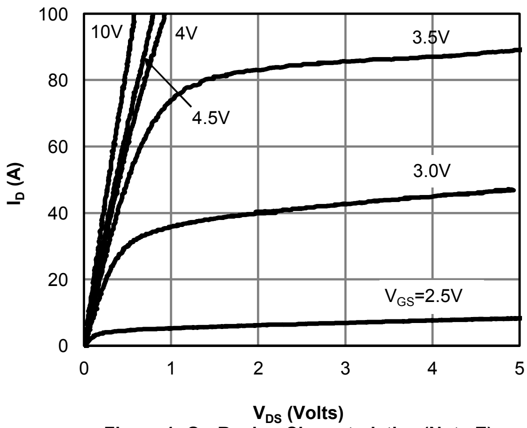


Figure 1: On-Region Characteristics (Note E)

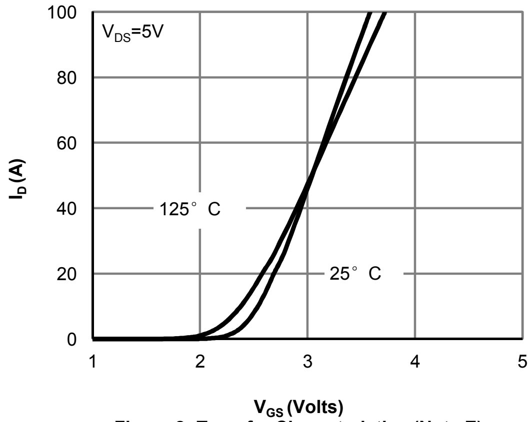


Figure 2: Transfer Characteristics (Note E)

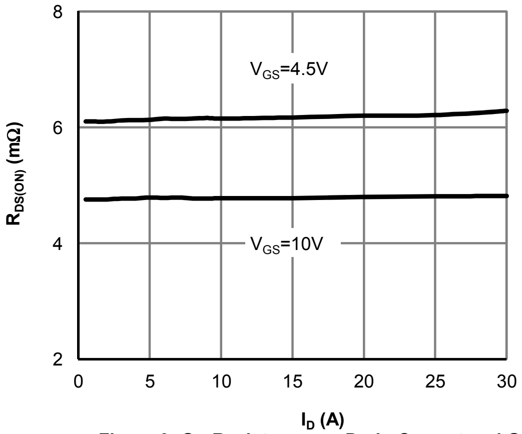


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

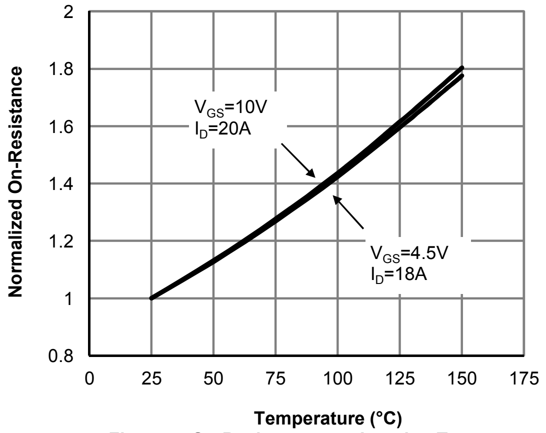


Figure 4: On-Resistance vs. Junction Temperature (Note E)

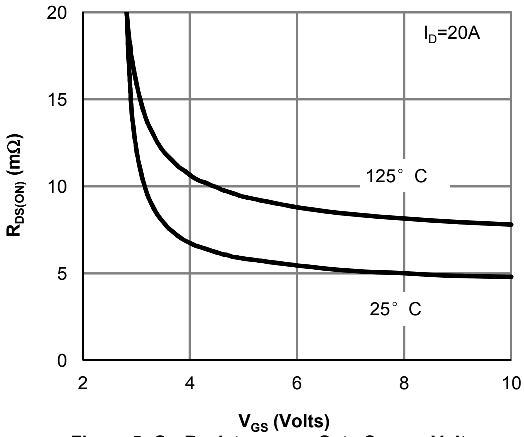


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

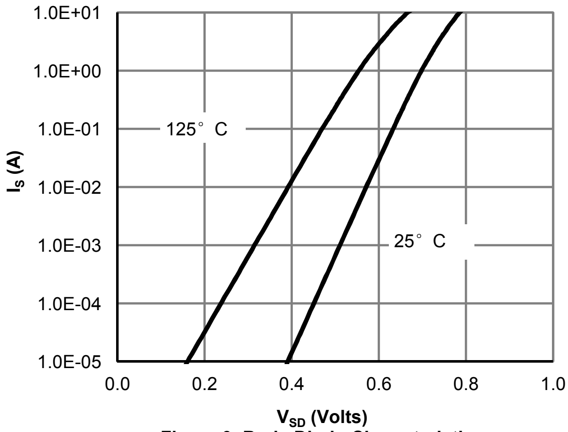


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

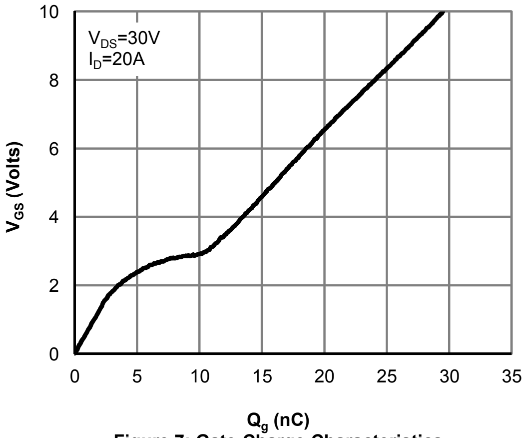


Figure 7: Gate-Charge Characteristics

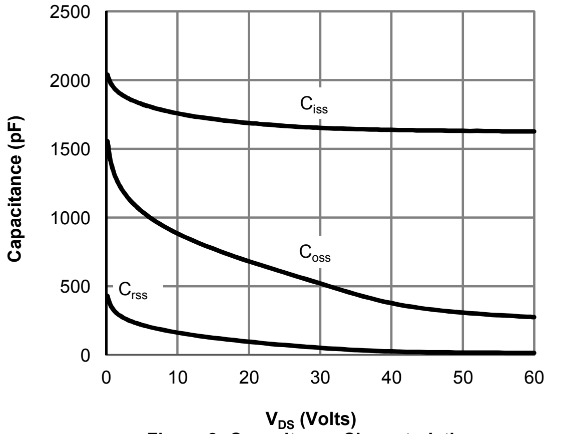
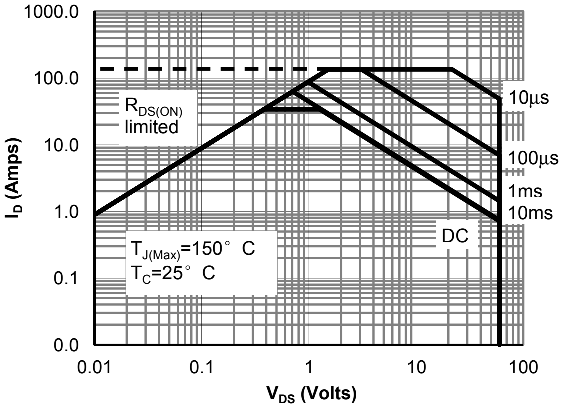


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

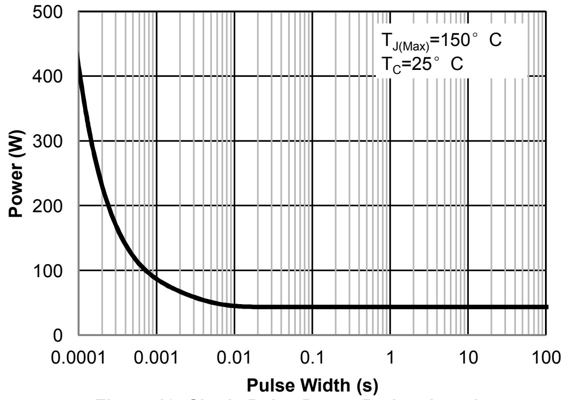


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

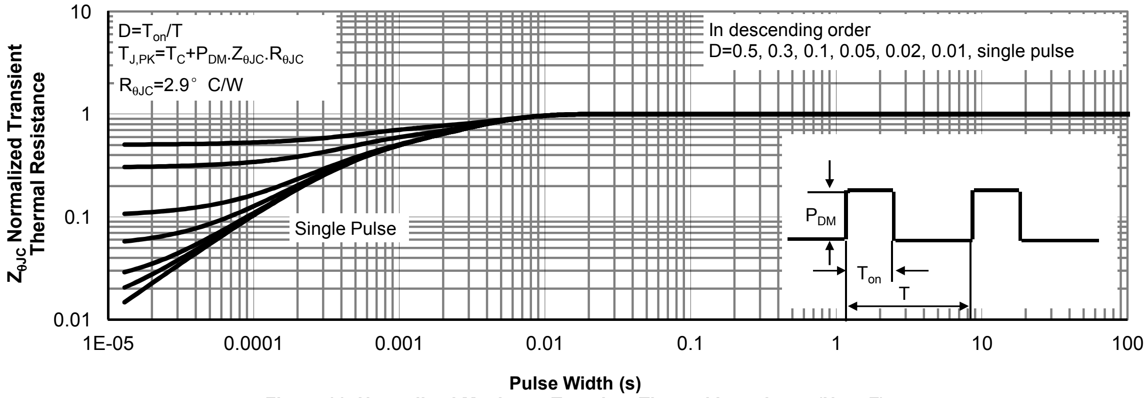


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

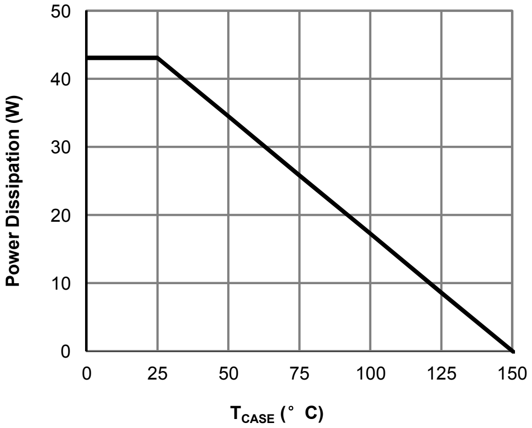


Figure 12: Power De-rating (Note F)

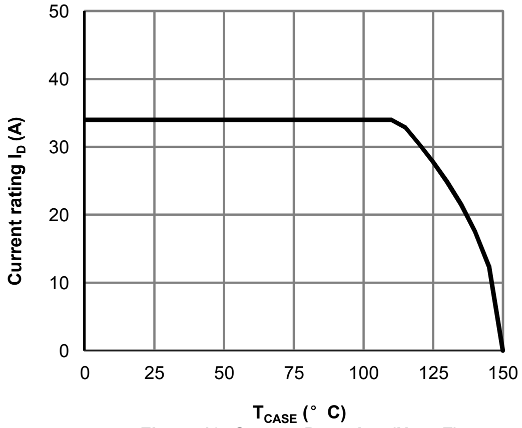


Figure 13: Current De-rating (Note F)

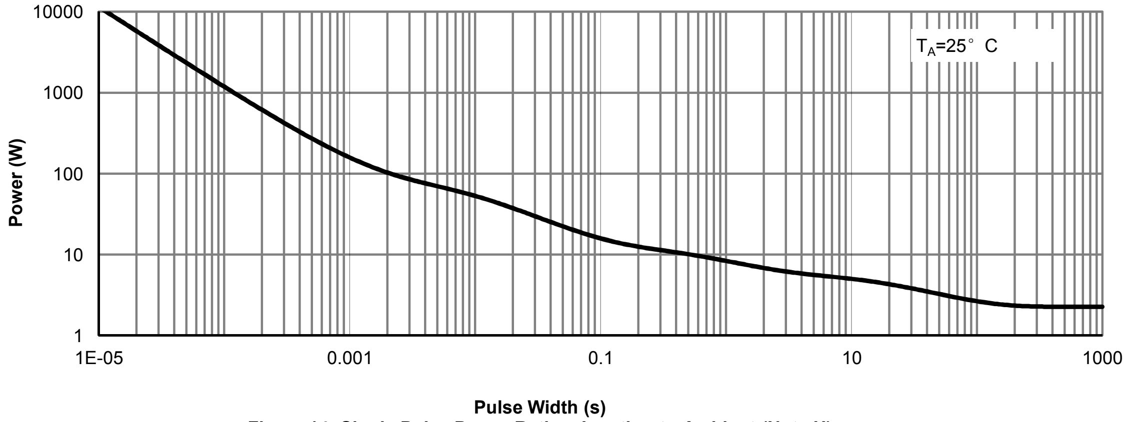


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

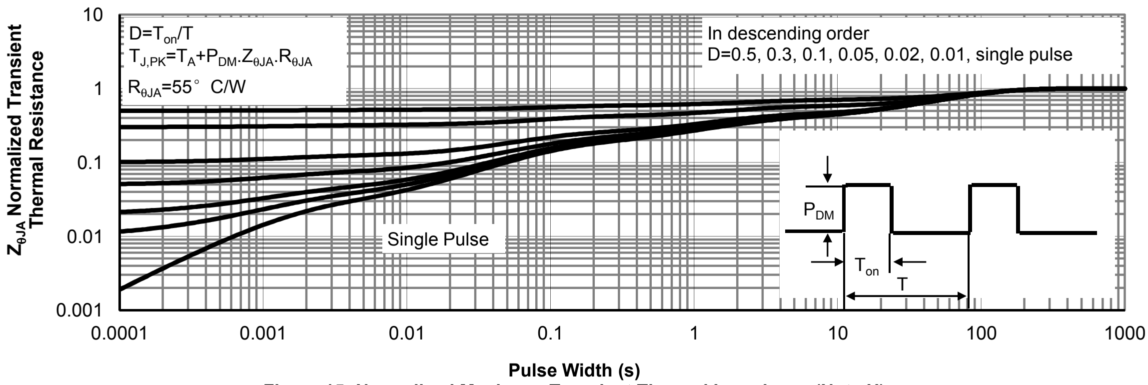


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

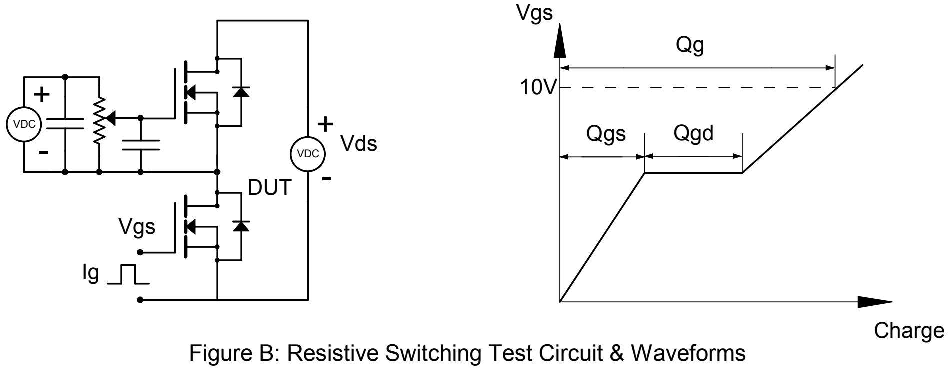


Figure B: Resistive Switching Test Circuit & Waveforms

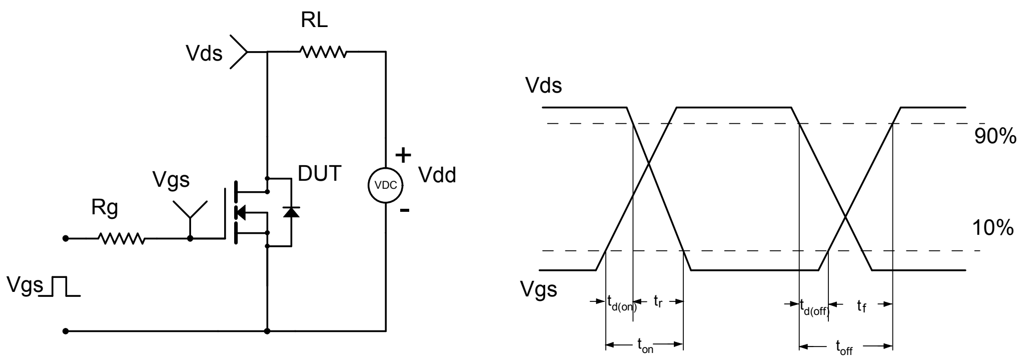


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

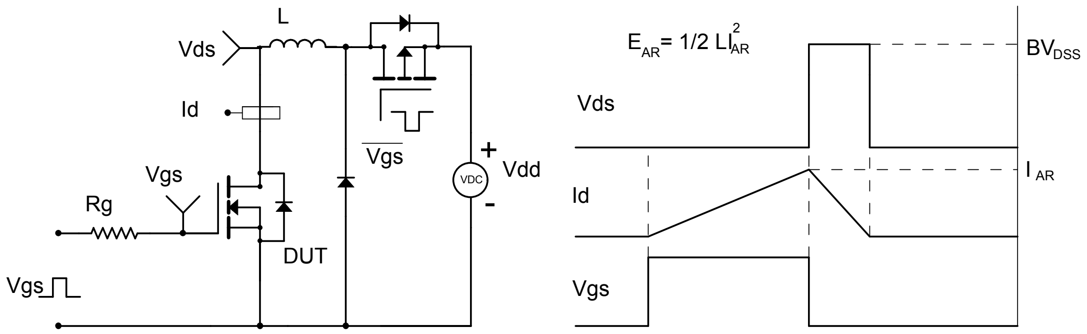


Figure D: Diode Recovery Test Circuit & Waveforms