

[www.maxim-ic.com](http://www.maxim-ic.com)

### GENERAL DESCRIPTION

The DS26502DK is an easy-to-use evaluation board for the DS26502 T1/E1/J1/64KCC BITS element. The DS26502DK is intended to be used as a stand-alone design kit. The board is complete with a DS26502 BITS element, transformers, termination resistors, FPGA-based configuration switches, and network connectors. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status as well as multiple clock and signal routing configurations.

*Windows* is a registered trademark of Microsoft Corp.

### DESIGN KIT CONTENTS

DS26502DK Design Kit

CD\_ROM Including:

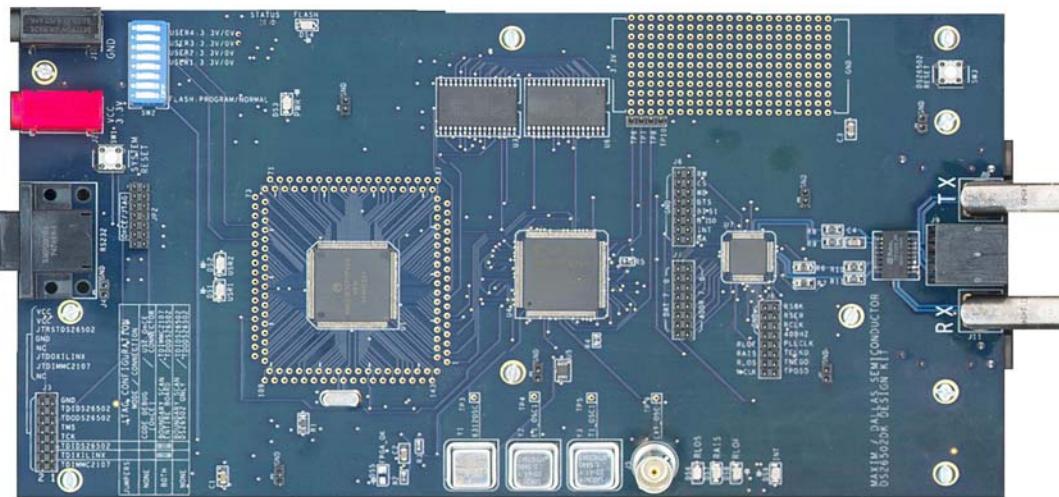
- ChipView Software
- DS26502DK Data Sheet
- DS26502 Data Sheet
- DS26502 Errata Sheet (if applicable)

### ORDERING INFORMATION

PART	DESCRIPTION
DS26502DK	Stand-Alone Design Kit for DS26502

### FEATURES

- **Expedites New Designs by Eliminating First-Pass Prototyping**
- **Demonstrates Key Functions of DS26502 BITS Element**
- **Includes DS26502 BITS Element, Transformers, BNC, and RJ48 Network Connectors and Termination Passives**
- **BNC Connections for 75Ω E1**
- **Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1**
- **Interface Directly to Windows-Based Computers**
- **ChipView Software Provides Point-and-Click Access to the DS26502 Register Set**
- **Software Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing**
- **All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal and Interrupt Status as well as Indications for Multiple Clock and Signal Routing Configurations**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

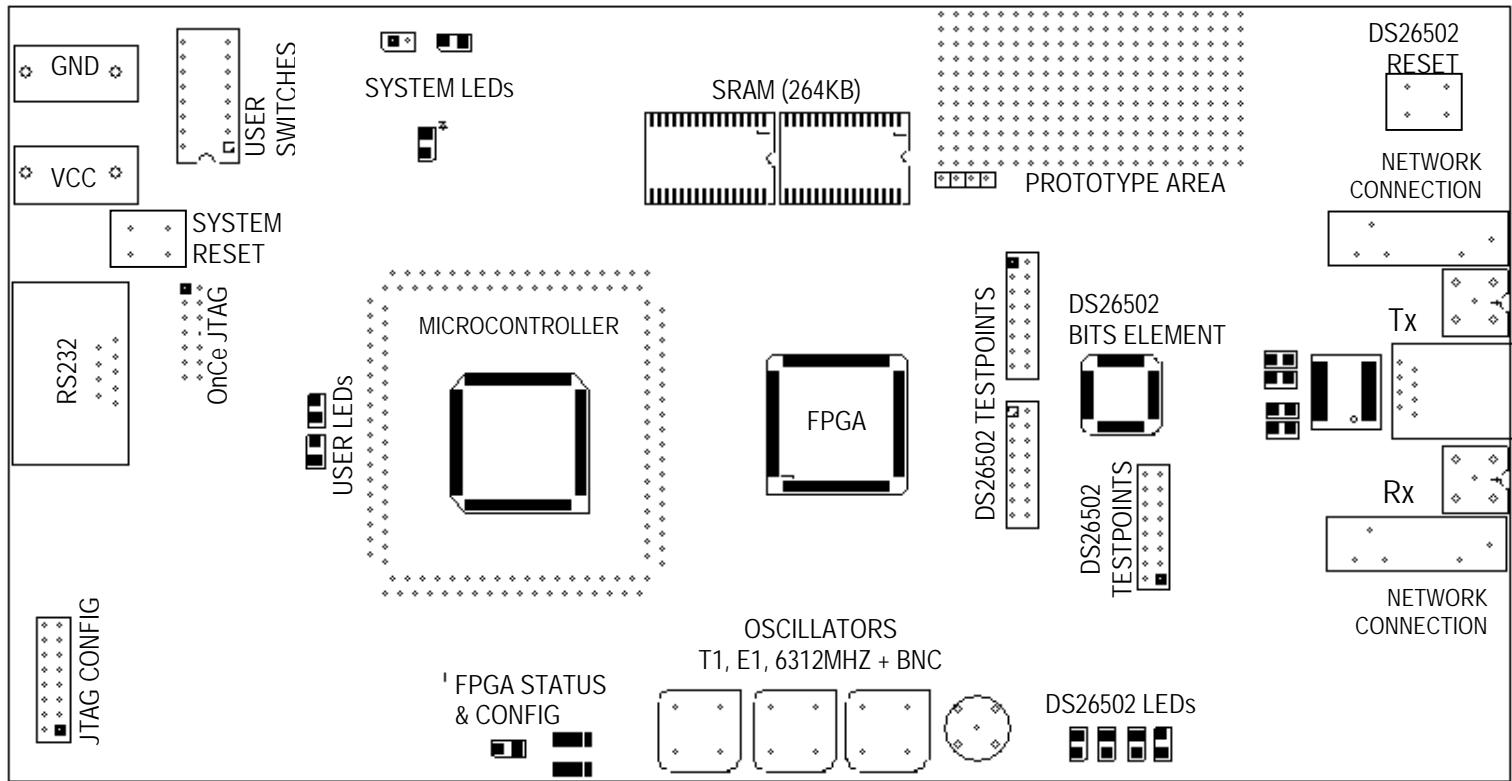


## COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C4, C23, C51, C53	5	10 $\mu$ F 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
C2–C3, C6–C9, C11, C12, C14, C15, C17, C18, C20, C21, C25–C30, C32, C33, C35, C36, C38, C45–C50, C52, C54, C55, C57–C60, C62, C63, C68	41	1 $\mu$ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C5, C10, C22, C24, C31, C34, C37, C39–C41, C43, C65–C67, C69, C70	16	0.1 $\mu$ F 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C13, C19, C42, C44, C64	5	10 $\mu$ F 20%, 16V tantalum capacitors (B case)	Panasonic	ECS-T1CX106R
C16, C56, C61	3	68 $\mu$ F 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
D1	1	1A 50V general-purpose silicon diode	General Semiconductor	1N4001
DS1, DS2, DS6–DS9	6	LED, RED, SMD	Panasonic	LN1251C
DS3	1	LED, GREEN, SMD	Panasonic	LN1351C
DS4	1	LED, AMBER, SMD	Panasonic	LN1451C
DS5	1	LED, GREEN, SMD (Not populated)	Panasonic	LN1351C
DS10	1	LED red/green, 5mm red/green right-angle PCMT	Digi-Key	350-1055-ND
J1	1	Socket, banana plug, horizontal, black	Mouser Electronics	164-6218
J2	1	Socket, banana plug, horizontal, red	Mouser Electronics	164-6219
J3, J6–J8	4	Terminal strip, 16-pin, dual row, vertical	Samtec	TSW-108-07-T-D
J4	1	DB9 right-angle, long case connector	AMP	747459-1
J5	1	L_CONNECTOR BNC 75 $\Omega$ vertical 5-pin	Cambridge	CP-BNCPC-004
J9	1	L_RJ48 8-pin, single-port connector	MOLEX	15-43-8588
J10, J11	2	BNC connectors, 75 $\Omega$ right-angle 5-pin	Kruvand	UCBJR220
J12, J13	2	L_CONN, Bantam jack, right-angle	Switchcraft	RTT34B02
JP1, JP3–JP8	7	100-mil, 2 position jumper	labstock	
JP2	1	14-pin header, remove 'missing pin'	labstock	
L1	1	Inductor, 22.0 $\mu$ H 2-pin SMT 20%	Coiltronics	UP1B-220
NP1, NP2	2	10pF 5%, 50V tall case ceramic capacitors (1206) Do not populate	Phycomp	1206CG100J9B200
R1, R8–R11	5	0 $\Omega$ 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R2, R13, R23, R27, R43, R47, R67–R70	10	330 $\Omega$ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R3, R18–R20, R22, R25, R26, R28–R31, R33–R42, R44–R46, R49, R50, R53, R56, R59, R61, R62, R65, R72	33	10kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R4, R5, R48, R51, R54, R55, R57, R58	8	30Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ300V
R6, R7	2	61.9Ω 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF61R9V
R12	1	51Ω 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ510V
R14–R17, R21, R24, R63, R64, R66, R71	10	1.0kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
R32	1	1.0kΩ 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ102V
R52	1	51.1Ω 1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF51R1V
R60	1	1.0MΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
SW1, SW3	2	Switch MOM 4-pin single pole	Panasonic	EVQPAE04M
SW2	1	Switch 8-position, 16-pin DIP, low profile	AMP	435668-7
T1	1	XFMR 16P SMT	Pulse	TX1099
TP1, TP2	2	Testpoint, 1 plate thru-hole	NA	NA
TP3–TP10	8	Testpoint, 1 plated hole DO NOT STUFF	NA	NA
U1	1	32-bit microcontroller (lab stock)	Avnet	MMC2107CFCV33
U3, U6	2	SRAM 5V, 1Mb SO (in lab stock)	Cypress	CY62128V
U4	1	Xilinx Spartan 2.5V FPGA, 20mm x 20mm 144-pin TQFP	Xilinx	XC2S50-5TQ144C
U5	1	8-Pin μMAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U7	1	64-pin LQFP T1/E1/J1 BITS element (0°C to +70°C)	Dallas Semiconductor	DS26502L
U8, U9, U13	3	High-speed inverter	Fairchild	NC7SZ86
U10	1	High-speed buffer	Fairchild	NC7SZ86
U11	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	Maxim	MAX3233E
U12	1	1Mb flash-based config mem	Xilinx	XCF01SV020C
U14	1	8-pin SO step-up DC-DC converter 0.5A limit	Maxim	MAX1675EUA
X1	1	Low-profile 8.0MHz crystal	PEI	EC1-8.000M
Y1	1	Oscillator, crystal clock, 3.3V, 6.312MHz	SaRonix	NTH069A3-6.312
Y2	1	Oscillator, crystal clock, 3.3V, 2.048MHz	SaRonix	NTH039A3-2.0480
Y3	1	Oscillator, crystal clock, 3.3V, 1.544MHz	SaRonix	NTH039A3-1.5440

## BOARD FLOORPLAN



## ERRATA

The design kit errata refer to two difference PC board revisions: the DS26502DK01A0 and DS26502DK01B0. The PC board revision code is found on the bottom of the board in the lower right corner.

### DS26502DK01A0 Circuit Boards

- RCLK did not get connected to FPGA. A jumper wire was run from RCLK to TP10 to provide the connection.
- Silkscreen for J3.4 is incorrect. Silkscreen reads “JTDIMMC2107” and should read “JTDOMMC2107.”
- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.
- DC blocking capacitor C4 on TTIP too small. A 10 $\mu$ F capacitor is recommended; a 1 $\mu$ F capacitor was populated.

### DS26502DK01B0 Circuit Boards

- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.

## ADDITIONS

The following signals have been connected to Testpoints via the FPGA:

- TP6 is driven with data present at the TS\_8K\_4 pin of the DS26502.
- TP7 is driven with the 400Hz signal mentioned in the TS\_8Ksrc register (page 15).
- TP8 is driven with the 8KHz signal mentioned in the TS\_8Ksrc register (page 15).

## BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at [www.maxim-ic.com/telecom](http://www.maxim-ic.com/telecom). See the DS26502DK QuickView data sheet for these files.

### ***Hardware Configuration***

- Supply 3.3V to the banana-plug receptacles marked GND and VCC\_3.3V.
- DIP switches are unused and can be in either the ON or OFF position with exception for the Flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

### **General**

- Upon power-up the RLOS and RLOF LEDs (red) will be lit, the INT LED (red) will not be lit, and Status LED (DS10 red/green bicolor) will be green.

### ***Quick Setup (Register View)***

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program will then request a definition file. Select DS26502DC\_FPGA.def. Through the ‘links’ section, this will also load DS26502.def.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS26502.
- Predefined Register settings for several functions are available as initialization files.
  - ini files are loaded by selecting the menu File→Reg ini File→Load ini File.
  - Load the ini file “CompositeClock.ini.”
  - Load the ini file “DS26502FPGA\_2048Clks.ini,” which sets the DS26502 in Intel nonmultiplexed mode with MCLK driven at 2.048MHz.
  - After loading the ini files the following may be observed:
    - The RLOS and RLOF LEDs extinguishes upon external loopback.
    - The part begins operating in composite clock mode.

### **Miscellaneous**

- Clock frequencies and certain pin bias levels are provided by a register-mapped FPGA.
- The definition file for this FPGA is named DS26502DC\_FPGA.def. The FPGA register definitions are located on page 6. A drop-down menu on the top of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the section marked “BASIC OPERATION.”

## ADDRESS MAP

Device address space (DS26502 and FPGA) begins at 0x81000000.

All offsets given below are relative to the beginning of the device address space (shown above).

**Table 1. Device Address Map**

OFFSET	DEVICE	DESCRIPTION
0x0000 to 0x0030	FPGA	Board identification and clock/signal routing
0x8000 to 0x80ff	DS26502 T1/E1/J1 BITS element	DS26502 T1/E1/J1 BITS element

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named “DS26502DC\_FPGA.def”.

## FPGA Register Map

**Table 2. FPGA Register Map**

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x0000	BID	Read only	BOARD ID
0x0001	Unused	—	—
0x0002	XBIDH	Read only	HIGH NIBBLE EXTENDED BOARD ID
0x0003	XBIDM	Read only	MIDDLE NIBBLE EXTENDED BOARD ID
0x0004	XBIDL	Read only	LOW NIBBLE EXTENDED BOARD ID
0x0005	BREV	Read only	BOARD FAB REVISION
0x0006	AREV	Read only	BOARD ASSEMBLY REVISION
0x0007	PREV	Read only	PLD REVISION
0x0007	BUSMO	Read only	BUS MODE INFORMATION
0x09-0x10	Unused	—	—
0x0011	LEVEL1	Control	DS26502 pin settings (THZE, BTS-HBE, BIS1, BIS0)
0x0012	LEVEL2	Control	DS26502 pin settings (RMODE3, RMODE2, RMODE1, RMODE0)
0x0013	LEVEL3	Control	DS26502 pin settings (RSM, RITD)
0x0014	LEVEL4	Control	DS26502 pin settings (TSM, TITD)
0x0015	LEVEL5	Control	DS26502 pin settings (TCSS1, TCSS0)
0x0016	LEVEL6	Control	DS26502 pin settings (TMODE3, TMODE2, TMODE1, TMODE0)
0x0017	LEVEL7	Control	DS26502 pin settings (L2, L1, L0)
0x0018	LEVEL8	Control	DS26502 pin settings (TAIS, RLB)
0x0019	LEVEL9	Control	DS26502 pin settings (MPS1, MPSO)
0x001A	LEVEL10	Control	DS26502 pin settings (JAMUX, E1TS)
0x001B	Unused	—	—
0x001C	TSERsrc	Control	DS26502 TSER source selection
0x001D	MCLKsrc	Control	DS26502 MCLK source selection
0x001E	TCLK	Control	DS26502 TCLK source selection
0x001F	TS_8K	Control	DS26502 TS_8K source selection
0x0020	Unused	—	—
0x0021	Unused	—	—

## FPGA ID Registers

### BID: BOARD ID (Offset = 0x0000)

BID is read only with a value of 0xD.

### XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0x0002)

XBIDH is read only with a value of 0x0.

### XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0x0003)

XBIDM is read only with a value of 0x1.

### XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0x0004)

XBIDL is read only with a value of 0x6.

### BREV: BOARD FAB REVISION (Offset = 0x0005).

BREV is read only and displays the current fab revision.

### AREV: BOARD ASSEMBLY REVISION (Offset = 0x0006)

AREV is read only and displays the current assembly revision.

### PREV: PLD REVISION (Offset = 0x0007)

PREV is read only and displays the current PLD firmware revision.

## FPGA Status Registers

Register Name: **BUSMO**

Register Description: **DS26502 Bus Mode**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	LevCPOL	LevCPHA	HW	SPI	INMUX	IMUX	MNMUX	MMUX
Default	—	—	—	—	—	—	—	—

The FPGA derives values in the BUSMO register from the levels present at the DS26502 pins.

**Bit 7: LevCPOL.** When set the DS26502 CPOL pin is high. Note: This pin is called A3/CPOL/L1 in parallel/serial/hardware modes.

**Bit 6: LevCPHA.** When set the DS26502 CPHA pin is high. Note: This pin is called A2/CPHA/L0 in parallel/serial/hardware modes.

**Bit 5: HW.** When set the DS26502 is in hardware mode.

**Bit 4: SPI.** When set the DS26502 is in SPI (3-wire) mode.

**Bit 3: INMUX.** When set the DS26502 is in Intel nonmultiplexed mode.

**Bit 2: IMUX.** When set the DS26502 is in Intel multiplexed mode.

**Bit 1: MNMUX.** When set the DS26502 is in Motorola nonmultiplexed mode.

**Bit 0: MMUX.** When set the DS26502 is in Motorola multiplexed mode.

## FPGA Control Registers

The FPGA register set consists of two types of registers: level setting and clock multiplexing. There are 10 registers for tri-state and level-control setting when in hardware mode. The level-setting registers are only valid when the DS26502 is in hardware mode (BIS1:0 = 11). When in nonhardware mode, the FPGA pins affected by the level registers are automatically either tri-stated, or assume an alternate function (e.g., they function as address databus pins or SPI pins). Exceptions are given with the register descriptions.

Register Name: **LEVEL1**

Register Description: **DS26502 Pin Settings (THZE, BTS, BIS1, BIS0)**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	THZEtri	THZE_Lev	BTStri	BTS_Lev	BIS1tri	BIS1_Lev	BIS0tri	BIS0_Lev
Default	0	0	0	0	0	0	0	1

**Note:** This register is only valid in ALL modes (many of the level registers are only valid in hardware mode).

### Bits 7 and 6: DS26502 THZE Tri-State and Level (THZEtri and THZE\_Lev)

- 00 = FPGA drives THZE with 0V
- 01 = FPGA drives THZE with 3.3V
- 1x = FPGA tri-states THZE pin

### Bit 5 and 4: DS26502 BTS Tri-State and Level (BTStri and BTS\_Lev)

- 00 = FPGA drives BTS with 0V
- 01 = FPGA drives BTS with 3.3V
- 1x = FPGA tri-states BTS pin

### Bits 3 and 2: DS26502 BIS1 Tri-State and Level (BIS1tri and BIS1\_Lev)

- 00 = FPGA drives BIS1 with 0V
- 01 = FPGA drives BIS1 with 3.3V
- 1x = FPGA tri-states BIS1 pin

### Bits 1 and 0: DS26502 BIS0 Tri-State and Level (BIS0tri and BIS0\_Lev)

- 00 = FPGA drives BIS0 with 0V
- 01 = FPGA drives BIS0 with 3.3V
- 1x = FPGA tri-states BIS0 pin

**Register Name: LEVEL2****Register Description: DS26502 Pin Settings (RMODE3, RMODE2, RMODE1, RMODE0)****Register Offset: 0x0012**

Bit #	7	6	5	4	3	2	1	0
Name	RMODE3 tri	RMODE3 _Lev	RMODE2 tri	RMODE2 _Lev	RMODE1 tri	RMODE1 _Lev	RMODE0 tri	RMODE0 _Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

**Bits 7 and 6: DS26502 RMODE3 Tri-State and Level (RMODE3tri and RMODE3\_Lev)**

00 = FPGA drives RMODE3 with 0V

01 = FPGA drives RMODE3 with 3.3V

1x = FPGA tri-states RMODE3 pin

**Bits 5 and 4: DS26502 RMODE2 Tri-State and Level (RMODE2tri and RMODE2\_Lev)**

00 = FPGA drives RMODE2 with 0V

01 = FPGA drives RMODE2 with 3.3V

1x = FPGA tri-states RMODE2 pin

**Bits 3 and 2: DS26502 RMODE1 Tri-State and Level (RMODE1tri and RMODE1\_Lev)**

00 = FPGA drives RMODE1 with 0V

01 = FPGA drives RMODE1 with 3.3V

1x = FPGA tri-states RMODE1 pin

**Bits 1 and 0: DS26502 RMODE0 Tri-State and Level (RMODE0tri and RMODE0\_Lev)**

00 = FPGA drives RMODE0 with 0V

01 = FPGA drives RMODE0 with 3.3V

1x = FPGA tri-states RMODE0 pin

**Register Name: LEVEL3****Register Description: DS26502 Pin Settings (RSM, RITD)****Register Offset: 0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RSMtri	RSM_Lev	—	—	RITDtri	RITD_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

**Bits 5 and 4: DS26502 RSM Tri-State and Level (RSMtri and RSM\_Lev)**

00 = FPGA drives RSM with 0V

01 = FPGA drives RSM with 3.3V

1x = FPGA tri-states RSM pin

**Bits 1 and 0: DS26502 RITD Tri-State and Level (RITDtri and RITD\_Lev)**

00 = FPGA drives RITD with 0V

01 = FPGA drives RITD with 3.3V

1x = FPGA Tristates RITD pin

**Register Name: LEVEL4****Register Description: DS26502 Pin Settings (TSM, TITD)****Register Offset: 0x0014**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TSMtri	TSM_Lev	—	—	TITDtri	TITD_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

**Bits 5 and 4: DS26502 TSM Tri-State and Level (TSMtri and TSM\_Lev)**

00 = FPGA drives TSM with 0V

01 = FPGA drives TSM with 3.3V

1x = FPGA tri-states TSM pin

**Bits 1 and 0: DS26502 TITD Tri-State and Level (TITDtri and TITD\_Lev)**

00 = FPGA drives TITD with 0V

01 = FPGA drives TITD with 3.3V

1x = FPGA tri-states TITD pin

**Register Name: LEVEL5****Register Description: DS26502 Pin Settings (TCSS1, TCSS0)****Register Offset: 0x0015**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TCSS1tri	TCSS1_Lev	—	—	TCSS0tri	TCSS0_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

**Bits 5 and 4: DS26502 TCSS1 Tri-State and Level (TCSS1tri and TCSS1\_Lev)**

00 = FPGA drives TCSS1 with 0V

01 = FPGA drives TCSS1 with 3.3V

1x = FPGA tri-states TCSS1 pin

**Bits 1 and 0: DS26502 TCSS0 Tri-State and Level (TCSS0tri and TCSS0\_Lev)**

00 = FPGA drives TCSS0 with 0V

01 = FPGA drives TCSS0 with 3.3V

1x = FPGA tri-states TCSS0 pin

**Register Name: LEVEL6****Register Description: DS26502 Pin Settings (TMODE3, TMODE2, TMODE1, TMODE0)****Register Offset: 0x0016**

Bit #	7	6	5	4	3	2	1	0
Name	TMODE3 tri	TMODE3 _Lev	TMODE2 tri	TMODE2 _Lev	TMODE1 tri	TMODE1 _Lev	TMODE0 tri	TMODE0 _Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.

**Bits 7 and 6: DS26502 TMODE3 Tri-State and Level (TMODE3tri and TMODE3\_Lev)**

00 = FPGA drives TMODE3 with 0V

01 = FPGA drives TMODE3 with 3.3V

1x = FPGA tri-states TMODE3 pin

**Bits 5 and 4: DS26502 TMODE2 Tri-State and Level (TMODE2tri and TMODE2\_Lev)**

00 = FPGA drives TMODE2 with 0V

01 = FPGA drives TMODE2 with 3.3V

1x = FPGA tri-states TMODE2 pin

**Bits 3 and 2: DS26502 TMODE1 Tri-State and Level (TMODE1tri and TMODE1\_Lev)**

00 = FPGA drives TMODE1 with 0V

01 = FPGA drives TMODE1 with 3.3V

1x = FPGA tri-states TMODE1 pin

**Bits 1 and 0: DS26502 TMODE0 Tri-State and Level (TMODE0tri and TMODE0\_Lev)**

00 = FPGA drives TMODE0 with 0V

01 = FPGA drives TMODE0 with 3.3V

1x = FPGA tri-states TMODE0 pin

**Register Name: LEVEL7****Register Description: DS26502 Pin Settings (L2, L1, L0)****Register Offset: 0x0017**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	L2tri	L2_Lev	L1tri	L1_Lev	L0tri	L0_Lev
Default	0	0	0	0	0	0	0	0

**Note:** Settings for L2 are only valid in hardware mode ( $BIS[1:0] = 11$ ), and ignored for other modes. In serial mode ( $BIS[1:0] = 10$ ), L0 and L1 are used to set levels for CPHA and CPOL, respectively.

**Bits 5 and 4: DS26502 L2 Tri-State and Level (L2tri and L2\_Lev)**

00 = FPGA drives L2 with 0V

01 = FPGA drives L2 with 3.3V

1x = FPGA tri-states L2 pin

**Bits 3 and 2: DS26502 L1 Tri-State and Level (L1tri and L1\_Lev)**

00 = FPGA drives L1 with 0V

01 = FPGA drives L1 with 3.3V

1x = FPGA tri-states L1 pin

**Bits 1 and 0: DS26502 L0 Tri-State and Level (L0tri and L0\_Lev)**

00 = FPGA drives L0 with 0V

01 = FPGA drives L0 with 3.3V

1x = FPGA tri-states L0 pin

**Register Name: LEVEL8****Register Description: DS26502 Pin Settings (TAIS, RLB)****Register Offset: 0x0018**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TAIS tri	TAIS_Lev	—	—	RLBtri	RLB_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 5 and 4: DS26502 TAIS Tri-State and Level (TAIS tri and TAIS\_Lev)**

00 = FPGA drives TAIS with 0V

01 = FPGA drives TAIS with 3.3V

1x = FPGA tri-states TAIS pin

**Bits 1 and 0: DS26502 RLB Tri-State and Level (RLBtri and RLB\_Lev)**

00 = FPGA drives RLB with 0V

01 = FPGA drives RLB with 3.3V

1x = FPGA tri-states RLB pin

**Register Name: LEVEL9****Register Description: DS26502 Pin Settings (MPS1, MPSO)****Register Offset: 0x0019**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	MPS1tri	MPS1_Lev	—	—	MPSOtri	MPSO_Lev
Default	0	0	0	0	0	0	0	0

**Bits 5 and 4: DS26502 MPS1 Tri-State and Level (MPS1tri and MPS1\_Lev)**

00 = FPGA drives MPS1 with 0V

01 = FPGA drives MPS1 with 3.3V

1x = FPGA tri-states MPS1 pin

**Bits 1 and 0: DS26502 MPS0 Tri-State and Level (MPSOtri and MPSO\_Lev)**

00 = FPGA drives MPS0 with 0V

01 = FPGA drives MPS0 with 3.3V

1x = FPGA tri-states MPS0 pin

**Register Name: LEVEL10****Register Description: DS26502 Pin Settings (JAMUX, E1TS)****Register Offset: 0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	JAMUXtri	JAMUX_Lev	—	—	E1TStri	E1TS_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode (BIS[1:0] = 11), and is ignored for other modes.**Bits 5 and 4: DS26502 JAMUX Tri-State and Level (JAMUXtri and JAMUX\_Lev)**

00 = FPGA drives JAMUX with 0V

01 = FPGA drives JAMUX with 3.3V

1x = FPGA tri-states JAMUX pin

**Bits 1 and 0: DS26502 E1TS Tri-State and Level (E1TStri and E1TS\_Lev)**

00 = FPGA drives E1TS with 0V

01 = FPGA drives E1TS with 3.3V

1x = FPGA tri-states E1TS pin

Register Name: **TSERsrc**

Register Description: **DS26502 TSER Pin Source**

Register Offset: **0x001C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	ZEROS	ONES	RSER
Default	0	0	0	0	0	0	1	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TSER. Setting to 0 also tri-states this pin.

**Bit 2: ZEROS.** When set DS26502\_TSER  $\leftarrow$  0.0V.

**Bit 1: ONES.** When set DS26502\_TSER  $\leftarrow$  3.3V.

**Bit 0: RSER.** When set DS26502\_TSER  $\leftarrow$  DS26502\_RSER.

Register Name: **MCLKsrc**

Register Description: **DS26502 MCLK Pin Source**

Register Offset: **0x001D**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	ZERO	EXT	T1	E1
Default	0	0	0	0	0	0	1	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to MCLK. Setting to 0 also tri-states this pin.

**Bit 3: ZERO.** When set DS26502\_MCLK  $\leftarrow$  0.0V.

**Bit 2: EXT.** When set DS26502\_MCLK  $\leftarrow$  External\_Osc (BNC connector).

**Bit 1: T1.** When set DS26502\_MCLK  $\leftarrow$  T1\_OSC (1.544MHz).

**Bit 0: E1.** When set DS26502\_MCLK  $\leftarrow$  E1\_OSC (2.048MHz).

Register Name: **TCLKsrc**

Register Description: **DS26502 TCLK Pin Source**

Register Offset: **0x001E**

Bit #	7	6	5	4	3	2	1	0
Name	—	EXT	T1	E1	64KHZ	6312	PLL	RCLK
Default	0	0	1	0	0	0	0	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TCLK. Setting to 0 also tri-states this pin.

**Bit 6: EXT.** When set DS26502\_ TCLK ← External\_Osc (BNC connector).

**Bit 5: T1.** When set DS26502\_ TCLK ← T1\_OSC (1.544MHz).

**Bit 4: E1.** When set DS26502\_ TCLK ← E1\_OSC (2.048MHz).

**Bit 3: 64KHZ.** When set DS26502\_ TCLK ← 64kHz clock.

**Bit 2: 6312.** When set DS26502\_ TCLK ← 6312kHz clock.

**Bit 1: PLL.** When set DS26502\_ TCLK ← DS26502\_PLL.

**Bit 0: RCLK.** When set DS26502\_ TCLK ← DS26502\_RCLK.

Register Name: **TS\_8Ksrc**

Register Description: **DS26502 TS\_8K Pin Source**

Register Offset: **0x001F**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	EXT	_8KHz	400HZ	400HZ_502	RS_8K
Default	0	0	0	0	0	0	1	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TS\_8K. Setting to 0 also tri-states this pin.

**Bit 4: EXT.** When set DS26502\_TS\_8K ← External\_Osc (BNC connector).

**Bit 3: \_8KHz.** When set DS26502\_TS\_8K ← 8kHz (derived by FPGA).

**Bit 2: 400HZ.** When set DS26502\_TS\_8K ← 400Hz clock (derived by FPGA).

**Bit 1: 4KHZ\_502.** When set DS26502\_TS\_8K ← DS26502\_400hz.

**Bit 0: RS\_8K.** When set DS26502\_TS\_8K ← DS26502\_RS\_8K.

## DS26502 INFORMATION

For more information about the DS26502, consult the DS26502 data sheet available on our website at [www.maxim-ic.com/DS26502](http://www.maxim-ic.com/DS26502). Software downloads are also available for this design kit.

## DS26502DK INFORMATION

For more information about the DS26502DK, including software downloads, consult the DS26502DK data sheet available on our website at [www.maxim-ic.com/DS26502DK](http://www.maxim-ic.com/DS26502DK).

## TECHNICAL SUPPORT

For additional technical support, go to [www.maxim-ic.com/support](http://www.maxim-ic.com/support).

## SCHEMATICS

The DS26502DK schematics are featured in the following pages.

## DOCUMENT REVISION HISTORY

REVISION DATE	DESCRIPTION
030705	Initial DS26502DK data sheet release.
070505	Updated <i>Features</i> , <i>Component List</i> (lines 1 and 2), and <i>Errata</i> sections.
071006	Updated descriptions for FPGA Control Registers LEVEL1 to LEVEL10.
110106	Updated schematics.
031507	Corrected typo on Bit 0 of TSERsrc register Corrected typo on Bit 0 of TS_8Ksrc register

- |   |   |   |   |
|---|---|---|---|
| A | B | C | D |
| B | 7 | 6 | 5 |
|   |   | 4 | 3 |
|   |   | 2 | 1 |
| B | 7 | 6 | 5 |
| 8 | 6 | 5 | 4 |
|   | 5 | 4 | 3 |
|   | 4 | 3 | 2 |
| 3 | 2 | 1 |   |
1. CONTENTS  
 2. DS26502 AND OSCILLATORS  
 3. DS26502 LINE BUILD OUT  
 4. XILINX CLOCK MUX AND BUS CONVERSION  
 5. TEST POINTS FOR DS26502  
 6. MMC2107 PROCESSOR  
 7. PROCESSOR CONFIGURATION  
 8. XILINX CONFIGURATION AND CORE VOLTAGE  
 9. SERIAL PORTS AND JTAG CONFIGURATION  
 10. MEMORY  
 11. PROCESSOR TEST POINTS  
 12. FLASH VOLTAGE AND DECOUPLING  
 13. SIGNAL CROSS REFERENCE  
 14. PART CROSS REFERENCE AND REVISION HISTORY

CONVERTED TO PDF: Fri Oct 20 10:08:32 2006

TITLE:	DS26502DK01B0	DATE:	041205
ENGINEER:	STEVE SCULLY	PAGE:	1 / 14

B 7 6 5 4 3 2 1

A D C B



1. 54MHz\_3.3V

Y3

OSC

Y3\_3

OUT

GND

C65

1UF

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

1

RTIP502  
RRING502RTIP  
RRINGRD#502  
CS#502  
WR#502  
BT502  
INT#50261  
60  
62  
55  
46RDX/  
DSK/  
WR#  
BT5/  
INT#/-/-/RMODE2  
/-/-/RMODE3  
/-/-/HBE  
INT\*/INT\*/JACKSTHZE502  
B1502  
B1510250  
59

THZE

B150

B151

MCLK

TCLK502

17

AD<0>/MISO/RMOSI  
AD<1>/MOSI/RMOSI  
AD<2>/SCLK/RSM  
AD<3>/-/TSM  
AD<4>/-/RMODE1  
AD<5>/-/RMODE2  
AD<6>/-/RITD  
AD<7>/-/RITD

RS\_BK502

26

RS\_BK

400HZ

R55

TSTRST502

39

TSTRST

TSER

TSER502

6

DAT502&lt;7..0&gt;

R57

PLL\_OUT

TCLKO

25

PLL\_CLK502

RCLK502

R58

RSER

28

RSER5502

R59

TNEG0502

TP050

R50

TP050502

R51

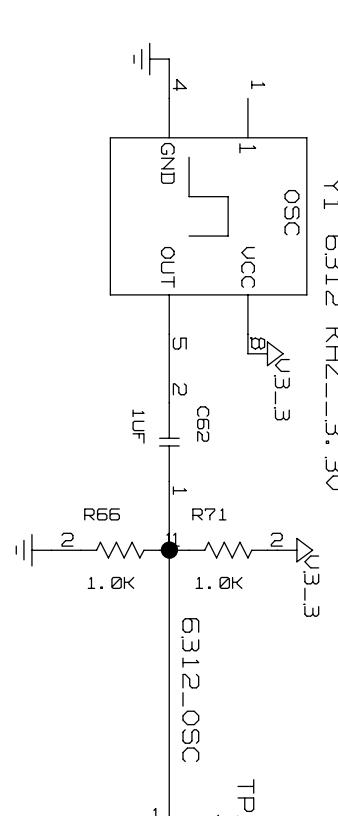
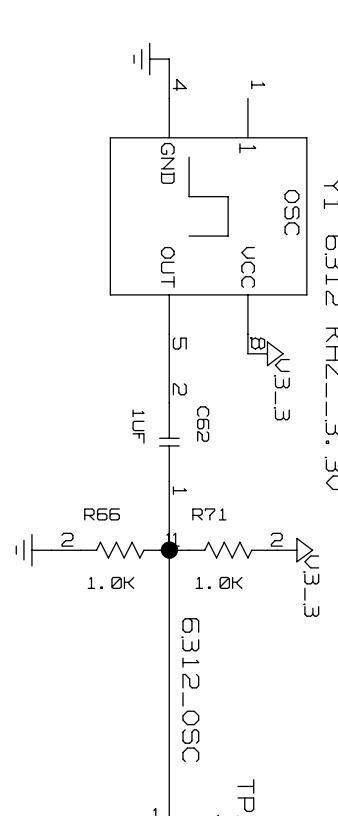
RA15502

R52

RLOF502

R53

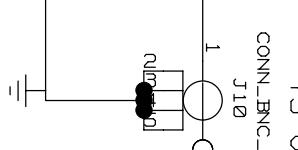
RLOF\_CCE



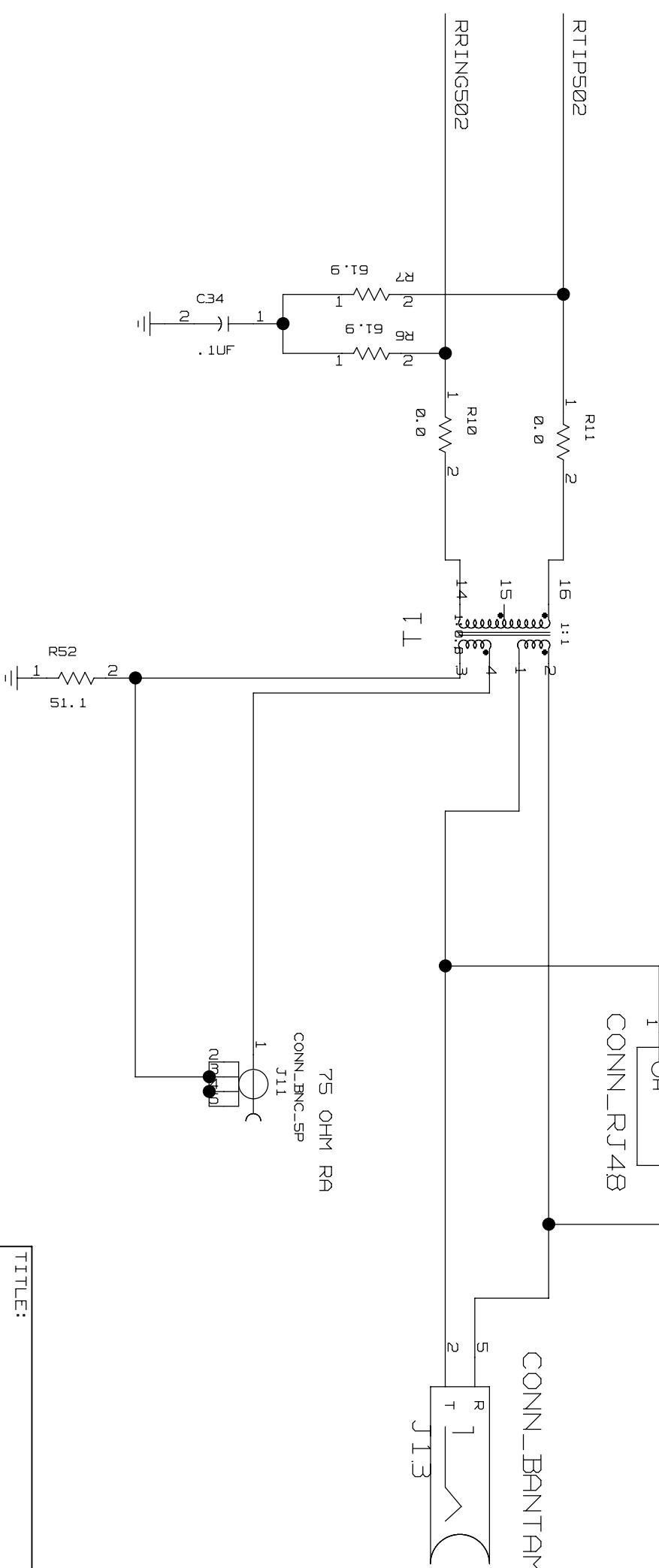
TITLE:	DS26502DK01B0
ENGINEER:	STEVE SCULLY

DATE:	041205
PAGE:	2 / 14

NOTE: THE DS26502DK01A0 CIRCUIT BOARDS USED A 1UF CAPACITOR (REFERENCE DESIGNATOR C4) FOR DC BLOCKING ON THE TTIP PIN. THIS HAS BEEN INCREASED TO 10UF ON THE DS26502DK01B0 CIRCUIT BOARDS



NOTE: BOARD REVISIONS DS26502DK01A0 AND DS26502DK01B0 DO NOT USE THE CORRECT PIN NUMBERS ON THE RJ48 CONNECTOR (REFERENCE DESIGNATOR J9). THE RJ48 CONNECTOR SHOULD BE REMOVED SINCE IT HAS NON-STANDARD CONNECTION. THE SCHEMATIC HAS BEEN UPDATED AND IS CORRECT.



B 7 6 5 4 3 2 1

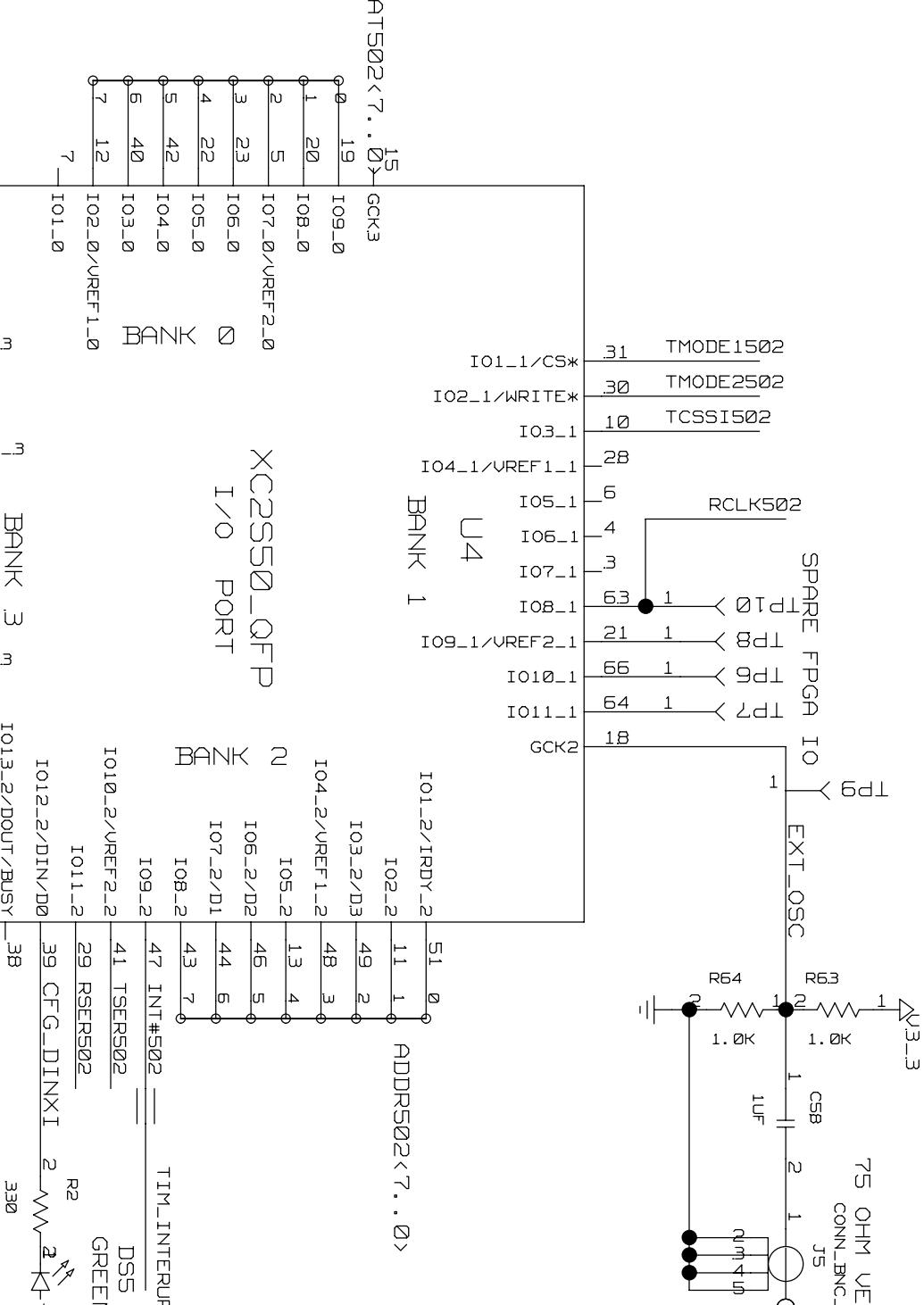
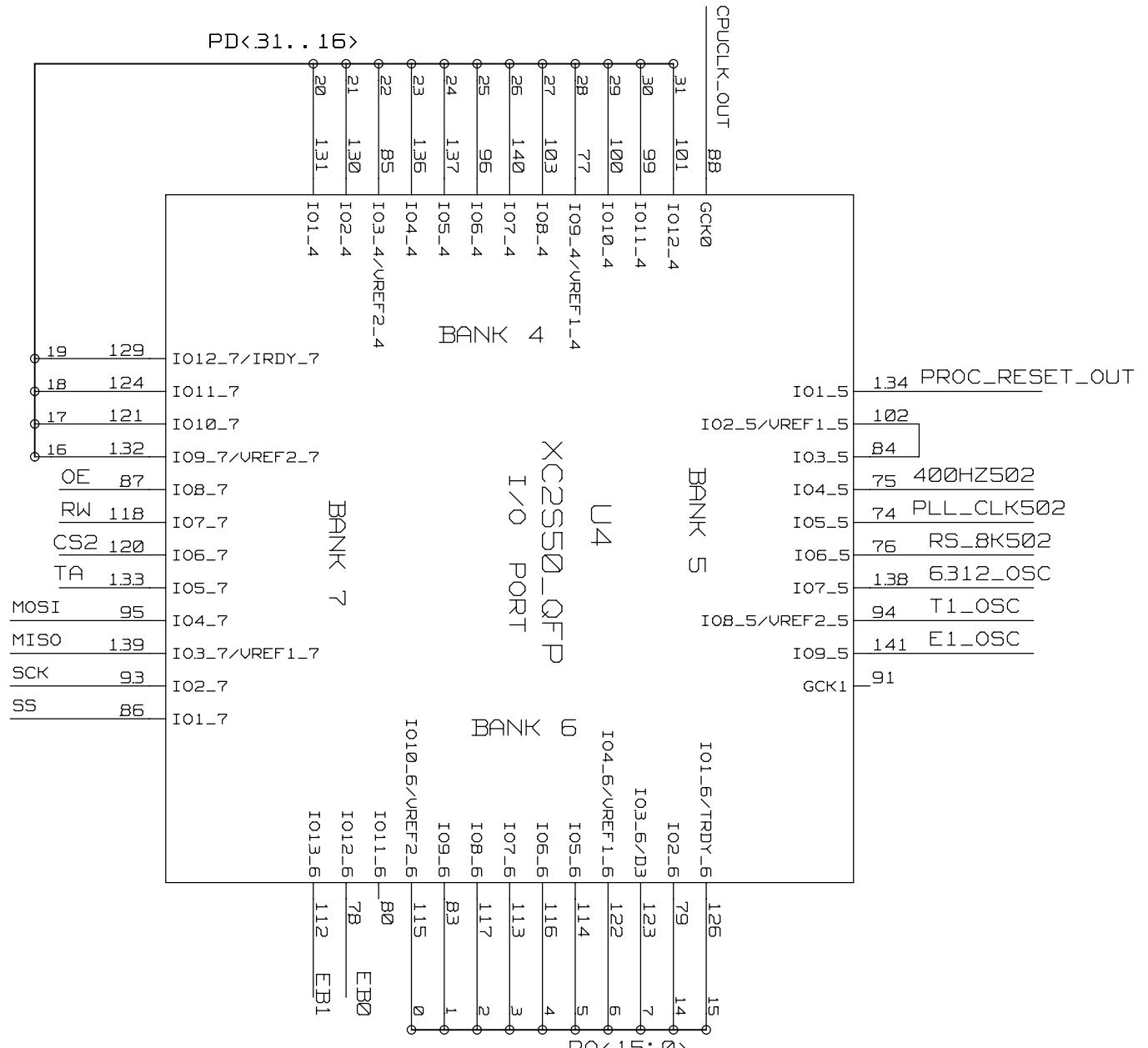
5 4 3

TITLE: DS26502DK01B0

DATE: 04/12/05

ENGINEER: STEVE SCULLY

PAGE: 3 / 14



This diagram illustrates the pinout and connection details for the DS26502DK01B0 FPGA board. It shows the following components and their connections:

- INPUTCLOCKS:** A vertical column of pins on the right side, labeled B at the top and bottom. Pins 7, 6, 5, 4, 3, and 2 are connected to ground (GND).
- CPUCLK\_OUT:** Pin 31 is connected to GCK0.
- PLL\_CLK502:** Pin 75 is connected to GCK1.
- RS\_8K502:** Pin 76 is connected to GCK1.
- 6312\_OSC:** Pin 138 is connected to GCK1.
- T1\_OSC:** Pin 94 is connected to GCK1.
- E1\_OSC:** Pin 141 is connected to GCK1.
- PROC\_RESET\_OUT:** Pin 134 is connected to GND.
- 400HZ502:** Pin 75 is connected to GND.
- PLL\_CLK502:** Pin 74 is connected to GND.
- RS\_8K502:** Pin 76 is connected to GND.
- 6312\_OSC:** Pin 138 is connected to GND.
- T1\_OSC:** Pin 94 is connected to GND.
- E1\_OSC:** Pin 141 is connected to GND.
- GND:** Pin 91 is connected to GND.

**Memory Banks:**

- BANK 5:** Contains XC2550\_QFP I/O PORT. Pins 30-31 are CPUCLK\_OUT\_BB and GCK0. Pins 29-30 are IO11\_4 and IO12\_4. Pins 28-29 are IO10\_4 and IO11\_4. Pin 28 is also labeled IO9\_4/VREF1\_4. Pin 27 is IO12\_7/IRDY\_7. Pin 26 is IO11\_7. Pin 25 is IO10\_7. Pin 24 is IO9\_7/VREF2\_7. Pin 23 is IO8\_7. Pin 22 is IO7\_7. Pin 21 is IO6\_7. Pin 20 is IO5\_7. Pin 19 is IO4\_7. Pin 18 is IO3\_7/VREF1\_7. Pin 17 is IO2\_7. Pin 16 is IO1\_7. Pin 15 is SS. Pin 14 is SCK. Pin 13 is TA. Pin 12 is CS2. Pin 11 is RW. Pin 10 is OE. Pin 9 is MOSI. Pin 8 is MISO. Pin 7 is SCK. Pin 6 is SS. Pin 5 is TA. Pin 4 is CS2. Pin 3 is RW. Pin 2 is OE. Pin 1 is MOSI.
- BANK 7:** Contains XC2550\_QFP I/O PORT. Pins 20-21 are IO12\_4/VREF2\_4. Pins 19-20 are IO11\_4 and IO12\_4. Pin 19 is IO12\_7/IRDY\_7. Pin 18 is IO11\_7. Pin 17 is IO10\_7. Pin 16 is IO9\_7/VREF2\_7. Pin 15 is IO8\_7. Pin 14 is IO7\_7. Pin 13 is IO6\_7. Pin 12 is IO5\_7. Pin 11 is IO4\_7. Pin 10 is IO3\_7/VREF1\_7. Pin 9 is IO2\_7. Pin 8 is IO1\_7.
- BANK 1:** Contains XC2550\_QFP I/O PORT. Pins 31-32 are IO1\_2/IRDY\_2 and IO2\_2. Pin 31 is IO1\_2/IRDY\_2. Pin 30 is IO2\_2. Pin 29 is IO3\_2/D3. Pin 28 is IO4\_1/VREF1\_1. Pin 27 is IO9\_1/VREF2\_1. Pin 26 is IO10\_1. Pin 25 is IO11\_1. Pin 24 is IO12\_6/VREF2\_6. Pin 23 is IO13\_6/VREF2\_6. Pin 22 is IO11\_6/VREF2\_6. Pin 21 is IO12\_6/VREF2\_6. Pin 20 is IO13\_6/VREF2\_6. Pin 19 is IO11\_6/VREF2\_6. Pin 18 is GCK2. Pin 17 is IO10\_2/VREF2\_2. Pin 16 is IO11\_2/VREF2\_2. Pin 15 is IO12\_2/DIN/D0. Pin 14 is IO13\_2/DOUT/BUSY. Pin 13 is IO1\_1/CS\*. Pin 12 is IO2\_1/WRITE\*. Pin 11 is IO3\_1. Pin 10 is IO4\_1/VREF1\_1. Pin 9 is IO5\_1. Pin 8 is IO6\_1. Pin 7 is IO7\_1. Pin 6 is IO8\_1. Pin 5 is IO9\_1/VREF2\_1. Pin 4 is IO10\_1. Pin 3 is IO11\_1. Pin 2 is IO12\_6/VREF2\_6. Pin 1 is IO13\_2/DOUT/BUSY.
- BANK 2:** Contains XC2550\_QFP I/O PORT. Pins 47-48 are TIM\_INTERRUPT and INT#502. Pin 47 is TIM\_INTERRUPT. Pin 46 is INT#502. Pin 45 is IO1\_2/IRDY\_2. Pin 44 is IO2\_2. Pin 43 is IO3\_2/D3. Pin 42 is IO4\_1/VREF1\_1. Pin 41 is IO5\_1. Pin 40 is IO6\_1. Pin 39 is IO7\_1. Pin 38 is IO8\_1. Pin 37 is IO9\_2. Pin 36 is IO10\_2/VREF2\_2. Pin 35 is IO11\_2/VREF2\_2. Pin 34 is IO12\_2/DIN/D0. Pin 33 is IO13\_2/DOUT/BUSY. Pin 32 is IO1\_1/CS\*. Pin 31 is IO2\_1/WRITE\*. Pin 30 is IO3\_1. Pin 29 is IO4\_1/VREF1\_1. Pin 28 is IO5\_1. Pin 27 is IO6\_1. Pin 26 is IO7\_1. Pin 25 is IO8\_1. Pin 24 is IO9\_2. Pin 23 is IO10\_2/VREF2\_2. Pin 22 is IO11\_2/VREF2\_2. Pin 21 is IO12\_2/DIN/D0. Pin 20 is IO13\_2/DOUT/BUSY. Pin 19 is IO1\_2/IRDY\_2. Pin 18 is IO2\_2.

**External Components:**

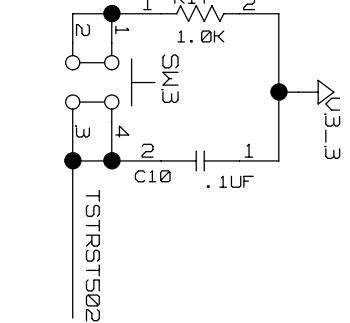
- RS232:** A circuit diagram for the RS232 port is shown on the right. It includes resistors R64 (1.0K), R63 (1.0K), and C5B (1uF). A 4-pin connector is labeled J5.
- EXT\_OSC:** A 7-pin connector labeled TP9 is connected to the EXT\_OSC pin.
- SPARE:** A 1-pin connector labeled TP10 is connected to the SPARE pin.
- FPGA:** A 14-pin connector labeled TP8 is connected to the FPGA pin.
- IO:** A 14-pin connector labeled TP9 is connected to the IO pin.

**Output Clocks:**

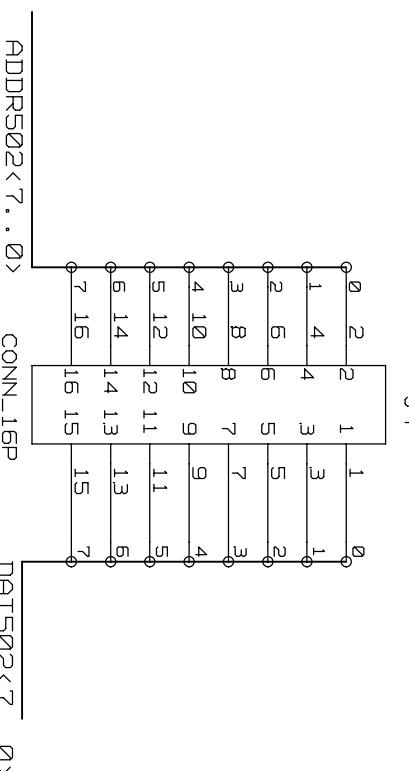
- MCLK502:** Pin 54 is IO13\_3/IRDY\_3. Pin 26 is IO12\_3. Pin 25 is IO11\_3/D4. Pin 24 is IO10\_3/VREF2\_3. Pin 23 is IO9\_3. Pin 22 is IO8\_3/D5. Pin 21 is IO7\_3/D6. Pin 20 is IO6\_3. Pin 19 is IO5\_3. Pin 18 is IO4\_3/VREF1\_3. Pin 17 is IO3\_3. Pin 16 is IO2\_3/D7. Pin 15 is IO1\_3/INITX.
- TCLK502:** Pin 57 is IO12\_3. Pin 56 is IO11\_3/D4. Pin 55 is IO10\_3/VREF2\_3. Pin 54 is IO9\_3. Pin 53 is IO8\_3/D5. Pin 52 is IO7\_3/D6. Pin 51 is IO6\_3. Pin 50 is IO5\_3. Pin 49 is IO4\_3/VREF1\_3. Pin 48 is IO3\_3. Pin 47 is IO2\_3/D7. Pin 46 is IO1\_3/INITX.
- TS\_8K\_4502:** Pin 58 is IO12\_3. Pin 57 is IO11\_3/D4. Pin 56 is IO10\_3/VREF2\_3. Pin 55 is IO9\_3. Pin 54 is IO8\_3/D5. Pin 53 is IO7\_3/D6. Pin 52 is IO6\_3. Pin 51 is IO5\_3. Pin 50 is IO4\_3/VREF1\_3. Pin 49 is IO3\_3. Pin 48 is IO2\_3/D7. Pin 47 is IO1\_3/INITX.
- THZE502:** Pin 27 is IO12\_3. Pin 26 is IO11\_3/D4. Pin 25 is IO10\_3/VREF2\_3. Pin 24 is IO9\_3. Pin 23 is IO8\_3/D5. Pin 22 is IO7\_3/D6. Pin 21 is IO6\_3. Pin 20 is IO5\_3. Pin 19 is IO4\_3/VREF1\_3. Pin 18 is IO3\_3. Pin 17 is IO2\_3/D7. Pin 16 is IO1\_3/INITX.
- RD#502:** Pin 60 is IO12\_3. Pin 59 is IO11\_3/D4. Pin 58 is IO10\_3/VREF2\_3. Pin 57 is IO9\_3. Pin 56 is IO8\_3/D5. Pin 55 is IO7\_3/D6. Pin 54 is IO6\_3. Pin 53 is IO5\_3. Pin 52 is IO4\_3/VREF1\_3. Pin 51 is IO3\_3. Pin 50 is IO2\_3/D7. Pin 49 is IO1\_3/INITX.
- CS#502:** Pin 62 is IO12\_3. Pin 61 is IO11\_3/D4. Pin 60 is IO10\_3/VREF2\_3. Pin 59 is IO9\_3. Pin 58 is IO8\_3/D5. Pin 57 is IO7\_3/D6. Pin 56 is IO6\_3. Pin 55 is IO5\_3. Pin 54 is IO4\_3/VREF1\_3. Pin 53 is IO3\_3. Pin 52 is IO2\_3/D7. Pin 51 is IO1\_3/INITX.
- WR#502:** Pin 59 is IO12\_3. Pin 58 is IO11\_3/D4. Pin 57 is IO10\_3/VREF2\_3. Pin 56 is IO9\_3. Pin 55 is IO8\_3/D5. Pin 54 is IO7\_3/D6. Pin 53 is IO6\_3. Pin 52 is IO5\_3. Pin 51 is IO4\_3/VREF1\_3. Pin 50 is IO3\_3. Pin 49 is IO2\_3/D7. Pin 48 is IO1\_3/INITX.
- BIS0502:** Pin 50 is IO12\_3. Pin 49 is IO11\_3/D4. Pin 48 is IO10\_3/VREF2\_3. Pin 47 is IO9\_3. Pin 46 is IO8\_3/D5. Pin 45 is IO7\_3/D6. Pin 44 is IO6\_3. Pin 43 is IO5\_3. Pin 42 is IO4\_3/VREF1\_3. Pin 41 is IO3\_3. Pin 40 is IO2\_3/D7. Pin 39 is IO1\_3/INITX.
- BIS1502:** Pin 65 is IO12\_3. Pin 64 is IO11\_3/D4. Pin 63 is IO10\_3/VREF2\_3. Pin 62 is IO9\_3. Pin 61 is IO8\_3/D5. Pin 60 is IO7\_3/D6. Pin 59 is IO6\_3. Pin 58 is IO5\_3. Pin 57 is IO4\_3/VREF1\_3. Pin 56 is IO3\_3. Pin 55 is IO2\_3/D7. Pin 54 is IO1\_3/INITX.
- BTS502:** Pin 56 is IO12\_3. Pin 55 is IO11\_3/D4. Pin 54 is IO10\_3/VREF2\_3. Pin 53 is IO9\_3. Pin 52 is IO8\_3/D5. Pin 51 is IO7\_3/D6. Pin 50 is IO6\_3. Pin 49 is IO5\_3. Pin 48 is IO4\_3/VREF1\_3. Pin 47 is IO3\_3. Pin 46 is IO2\_3/D7. Pin 45 is IO1\_3/INITX.
- X\_INITXI:** Pin 67 is IO12\_3. Pin 66 is IO11\_3/D4. Pin 65 is IO10\_3/VREF2\_3. Pin 64 is IO9\_3. Pin 63 is IO8\_3/D5. Pin 62 is IO7\_3/D6. Pin 61 is IO6\_3. Pin 60 is IO5\_3. Pin 59 is IO4\_3/VREF1\_3. Pin 58 is IO3\_3. Pin 57 is IO2\_3/D7. Pin 56 is IO1\_3/INITX.

**502 BUS MODE DETECTION:**

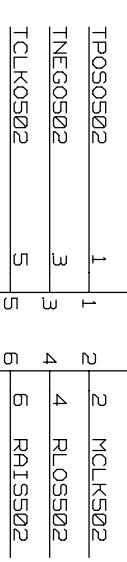
TITLE: DS26502DK01B0	DATE: 041205
ENGINEER: STEVE SCULLY	PAGE: 4 / 14



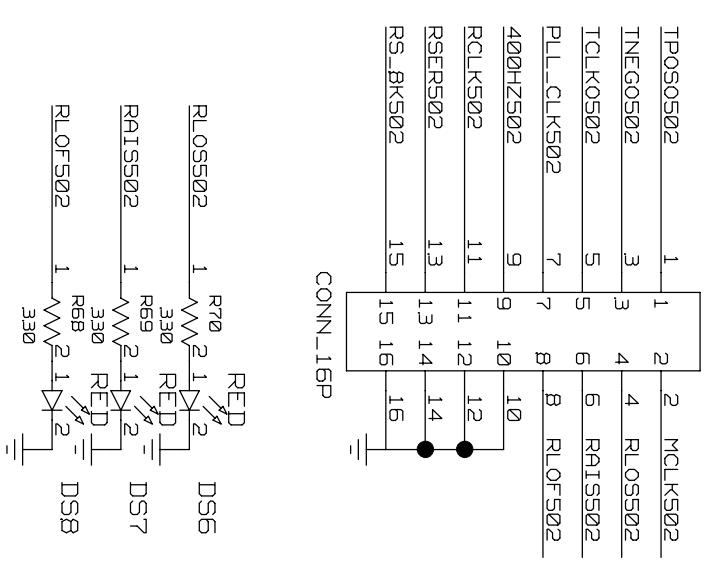
J7  
B 7 6 5 4 3 2 1



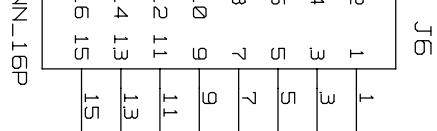
J7  
B 7 6 5 4 3 2 1



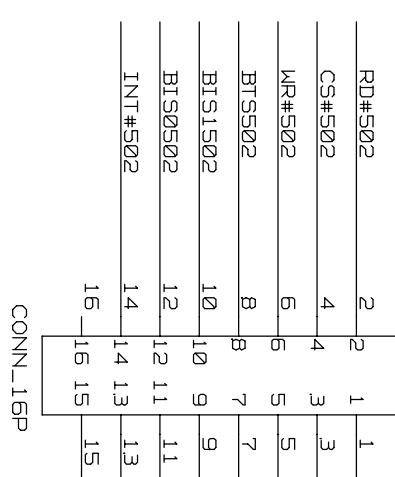
J8



J8

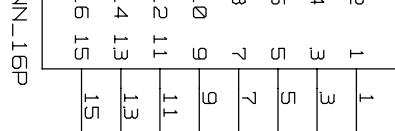


J6

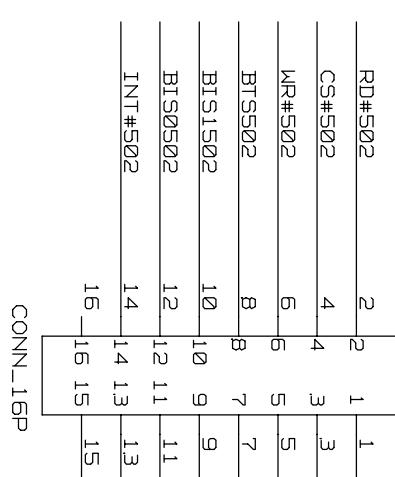


J6

J6

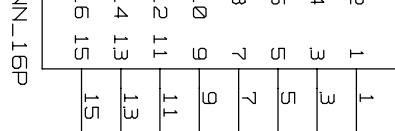


J5

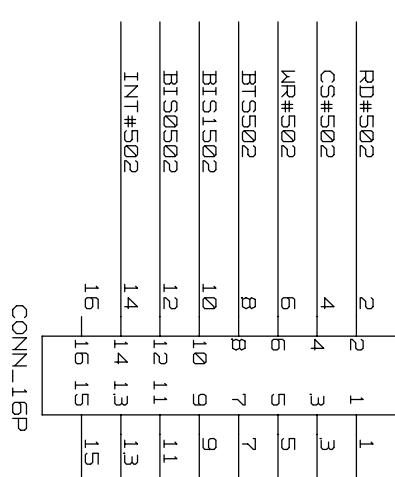


J5

J5

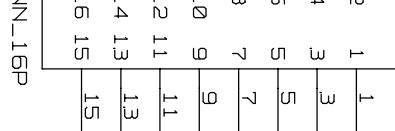


J4

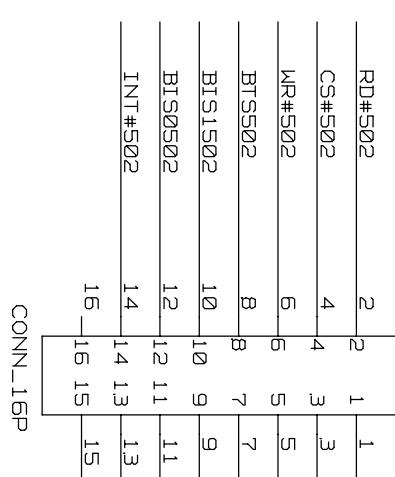


J4

J4

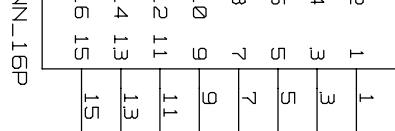


J3

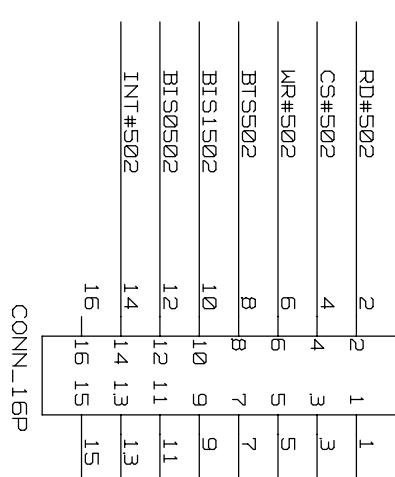


J3

J3

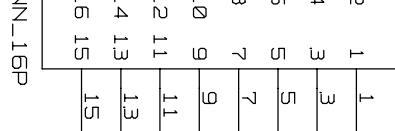


J2

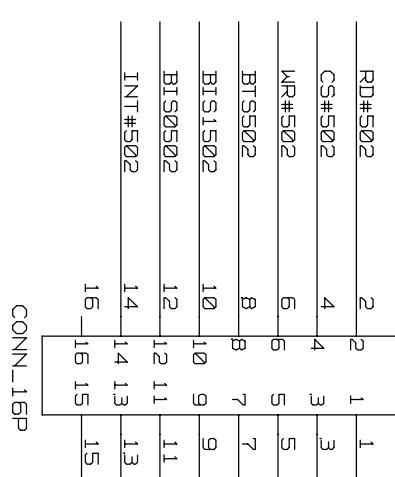


J2

J2

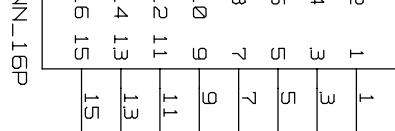


J1

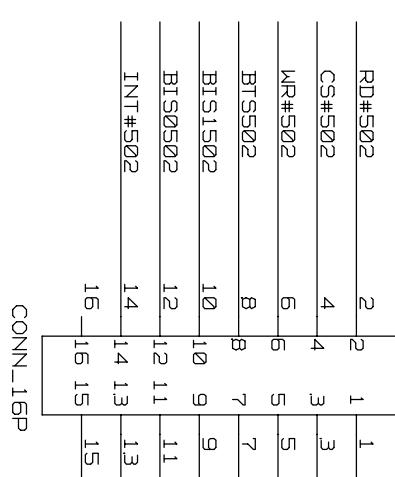


J1

J1

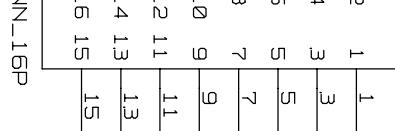


J0

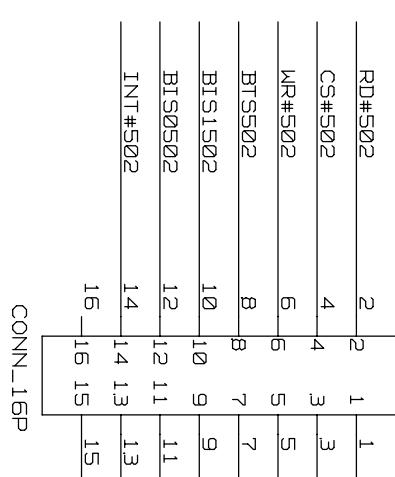


J0

J0

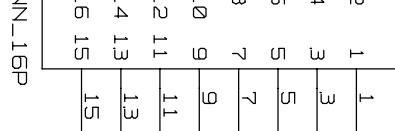


J-

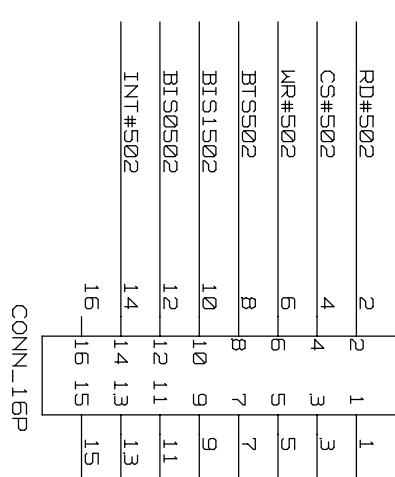


J-

J-

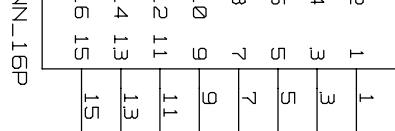


J+

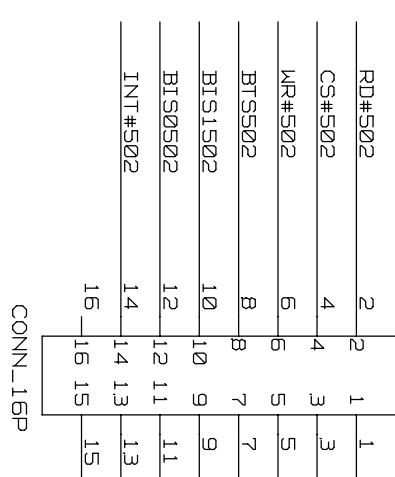


J+

J+

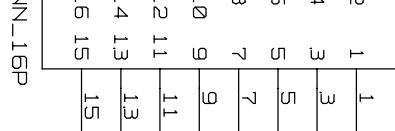


J-

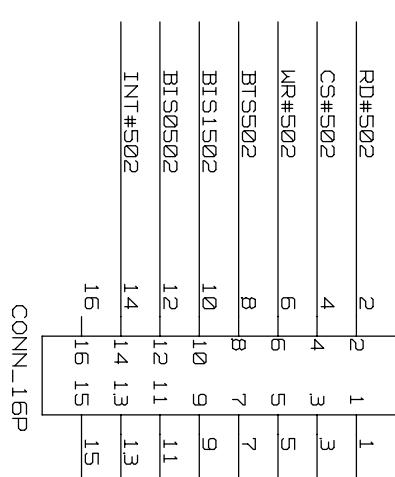


J-

J-

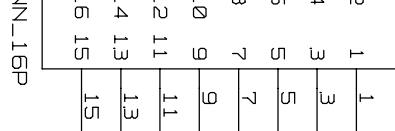


J+

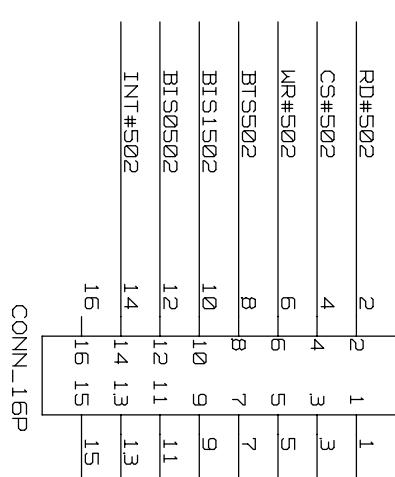


J+

J+

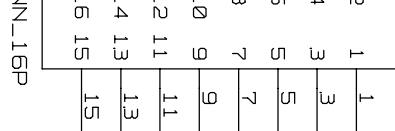


J-

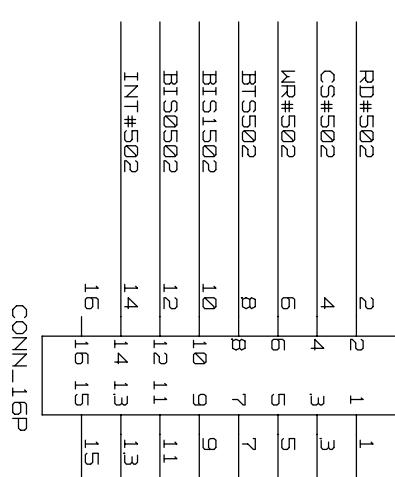


J-

J-

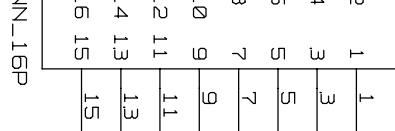


J+

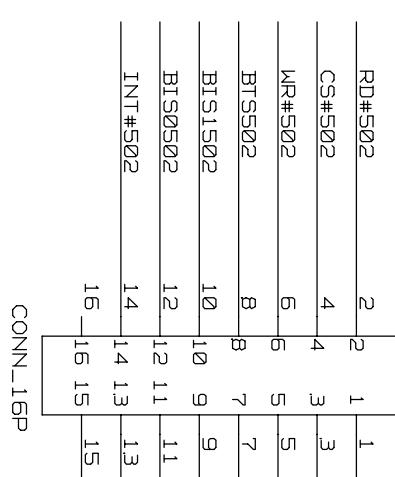


J+

J+

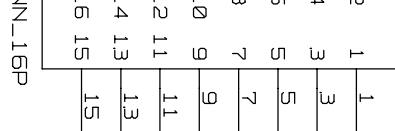


J-

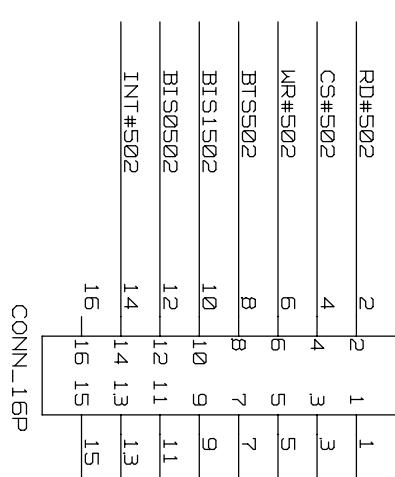


J-

J-

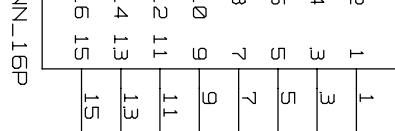


J+

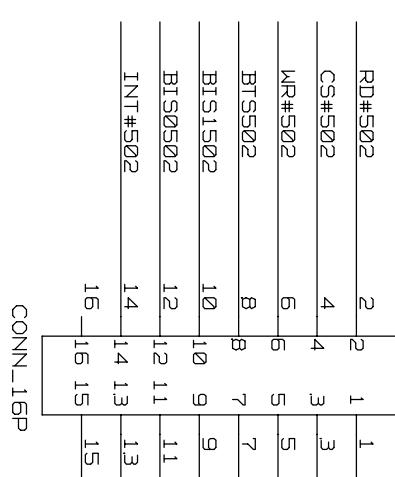


J+

J+

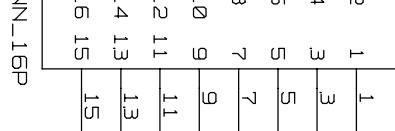


J-

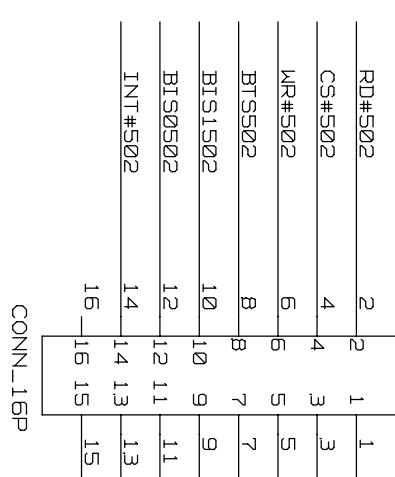


J-

J-

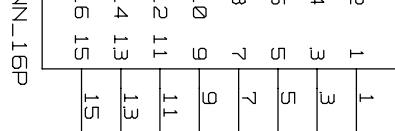


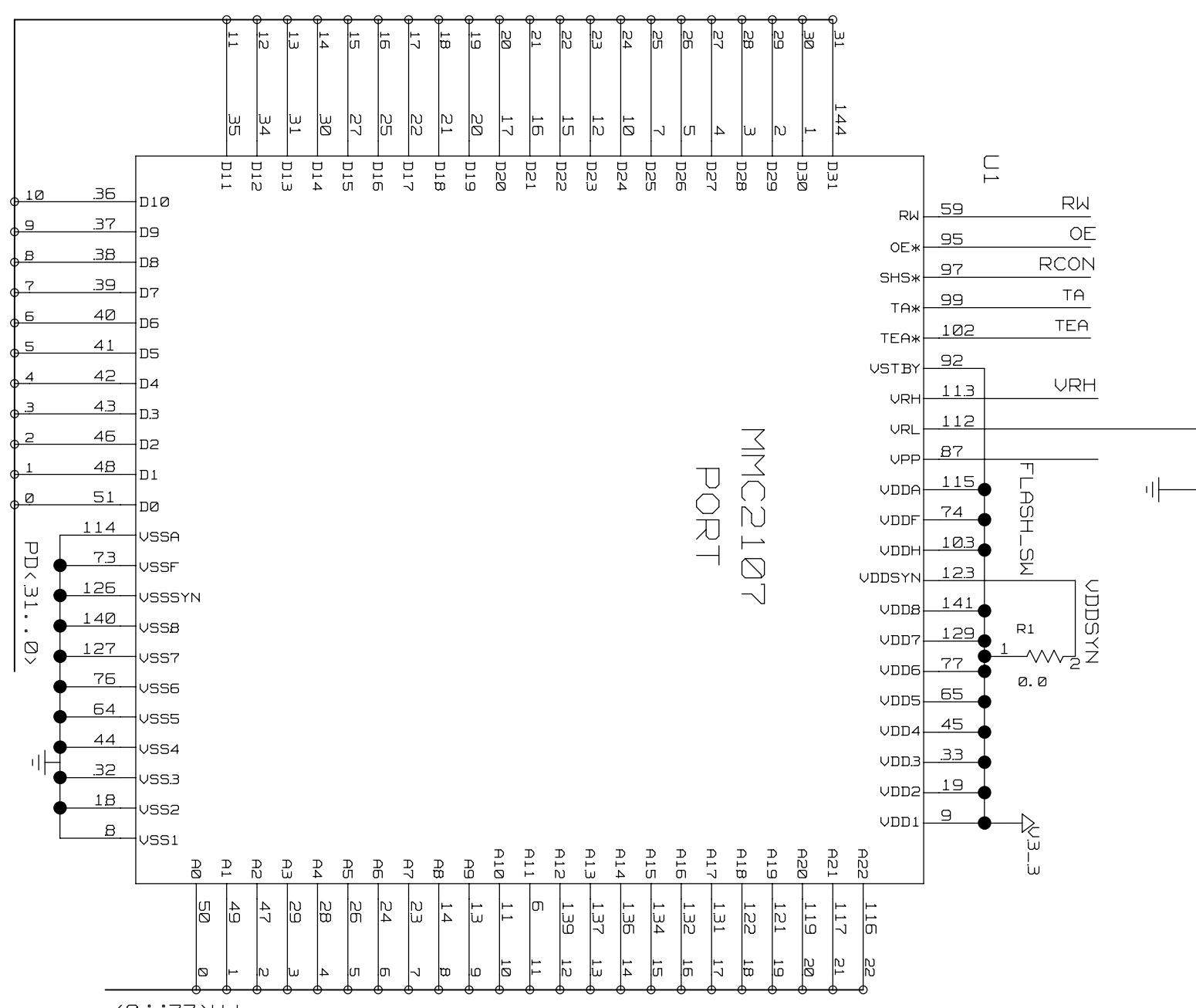
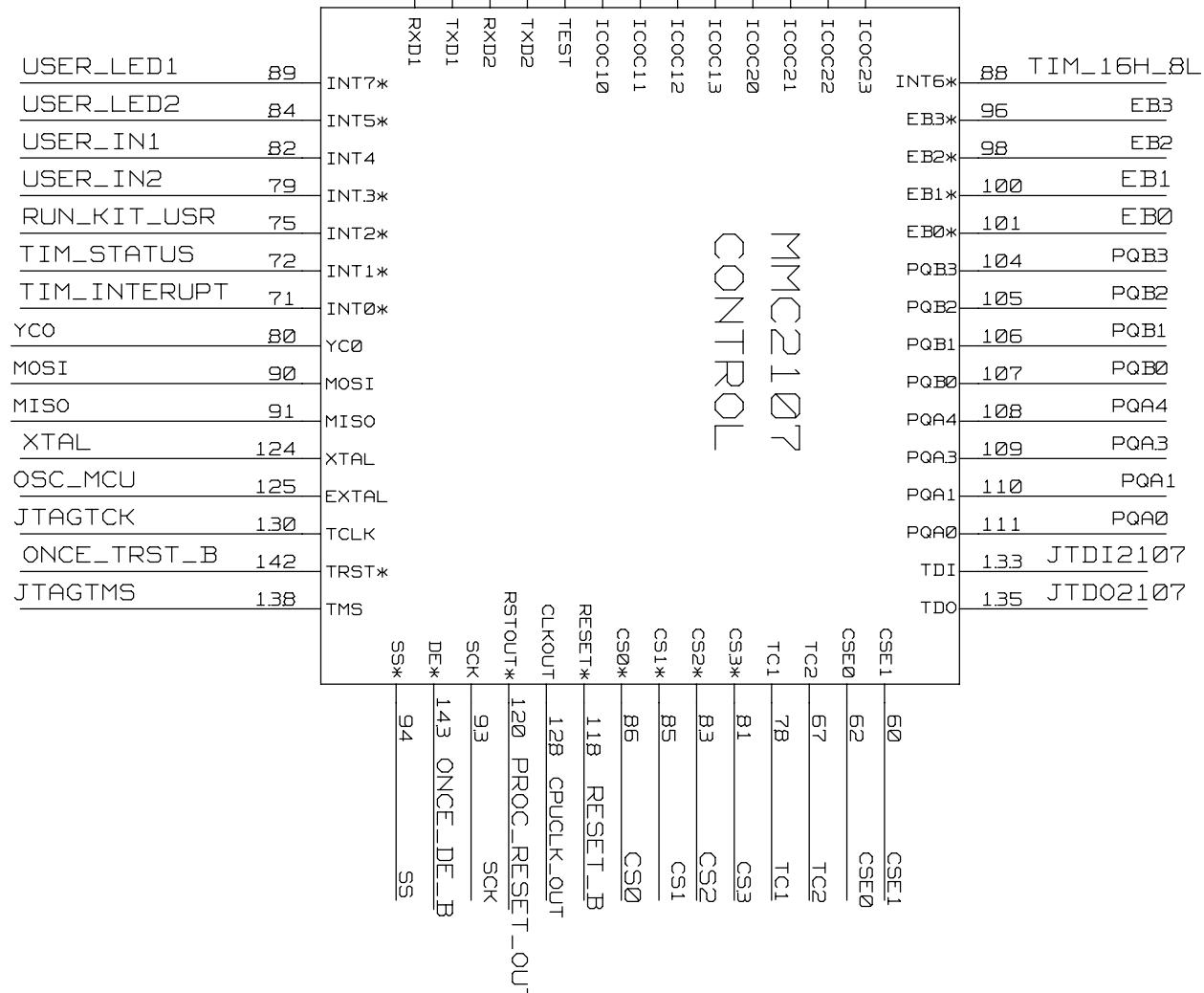
J+



J+

J+





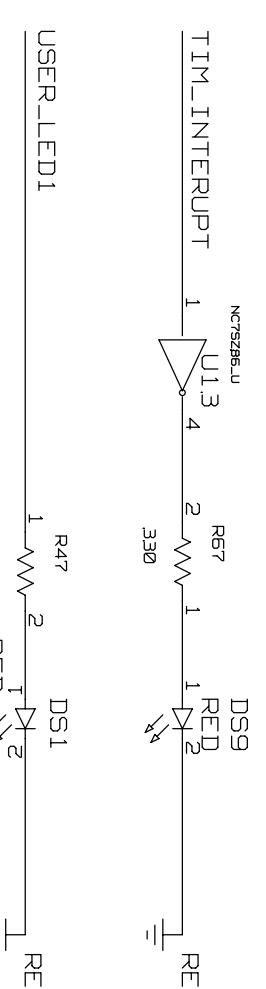
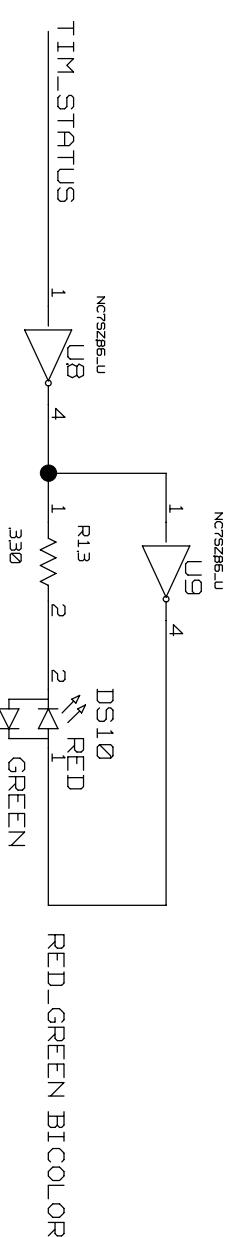
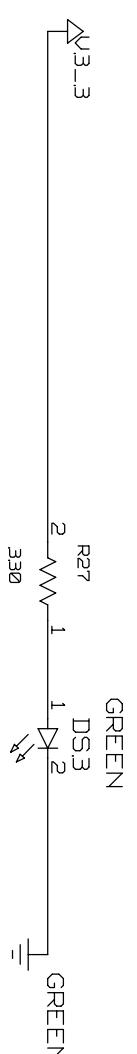
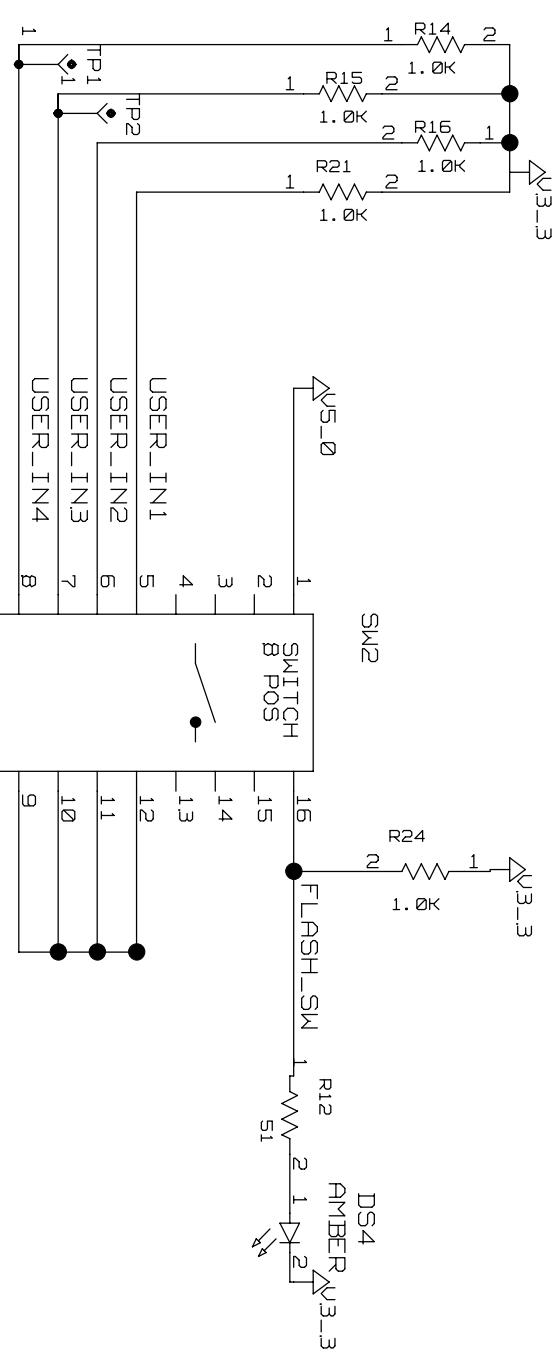
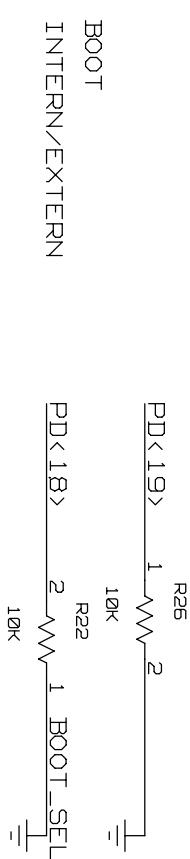
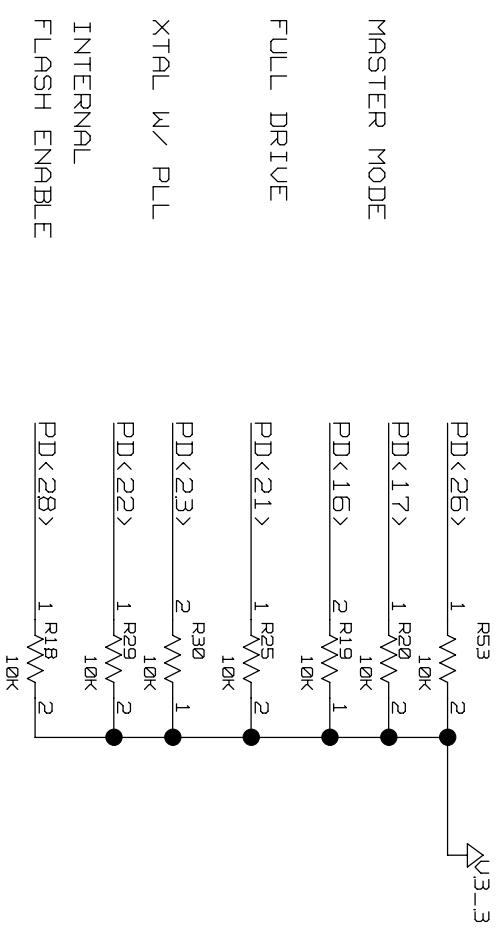
**U1**

ICOC23	52	ICOC23	31	144	D31
ICOC22	53	ICOC22	30	1	D30
ICOC21	54	ICOC21	29	2	D29
ICOC20	55	ICOC20	28	3	D28
ICOC13	56	ICOC13	27	4	D27
ICOC12	57	ICOC12	26	5	D26
ICOC11	58	ICOC11	25	7	D25
ICOC10	61	ICOC10	24	10	D24
GND	—TEST 63	TEST	23	12	D23
SCI2_OUT	65	TxD2	22	15	D22
SCI2_IN	68	RxD2	21	16	D21
SCI1_OUT	69	TxD1	20	17	D20
SCI1_IN	70	RxD1	19	20	D19
			18	21	D18
			17	22	D17
			16	25	D16
			15	27	D15
			14	30	D14
			13	31	D13
			12	34	D12
			11	35	D11
			10	36	D10
			9	37	D9
			8	38	D8
			7	39	D7
			6	40	D6
			5	41	D5
			4	42	D4
			3	43	D3
			2	46	D2
			1	48	D1
			0	51	D0
		VSSA	114		
		VSSF	73		
		VSSYN	126		
		VSS8	140		
		VSS7	127		
		VSS6	76		
		VSS5	64		
		VSS4	44		
		VSS3	32		
		VSS2	18		
		VSS1	8		

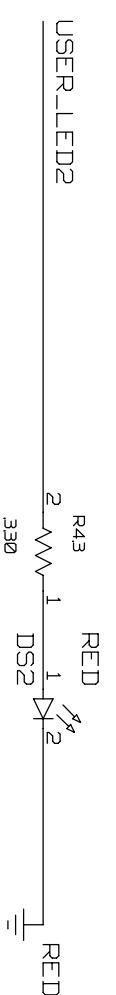
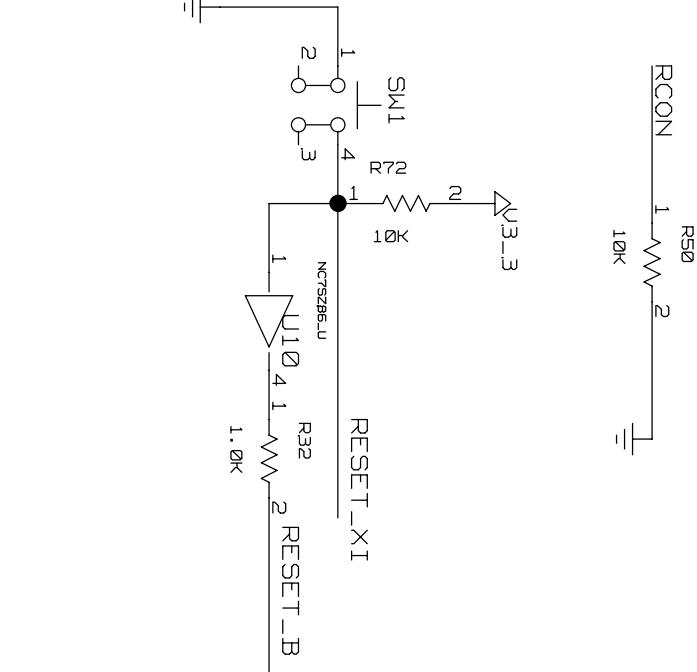
**U2**

INT6*	88	TIM_16H_8L	RW
EB3*	96	EB3	OE*
EB2*	98	EB2	RCON
EB1*	100	EB1	TA
EB0*	101	EB0	TEA
PQB3	104	PQB3	VSTBY
PQB2	105	PQB2	VRH
PQB1	106	PQB1	FLASH_SW
PQB0	107	PQB0	VRL
PQA4	108	PQA4	VPP
PQA3	109	PQA3	VDDA
PQA1	110	PQA1	VDDF
PQA0	111	PQA0	VDDH
TDI	133	JTDI2107	VDDSYN
TDO	135	JTDO2107	VDD8
CSE1	60	CSE1	VDD7
CSE0	62	CSE0	VDD6
TC2	67	TC2	VDD5
TC1	78	TC1	VDD4
CS3*	81	CS3	VDD3
CS2*	83	CS2	VDD2
CS1*	85	CS1	VDD1
CS0*	86	CS0	
RESET*	118	RESET_B	
CLKOUT	128	CPUCLK_OUT	
RSTOUT*	120	PROC_RESET_OUT	
SCK	93	SCK	
DE*	143	ONCE_DE_B	
SS*	94	SS	

## RESET CONFIGURATION



RESET AND CHIP CONFIGURATION



B 7 6 5 4

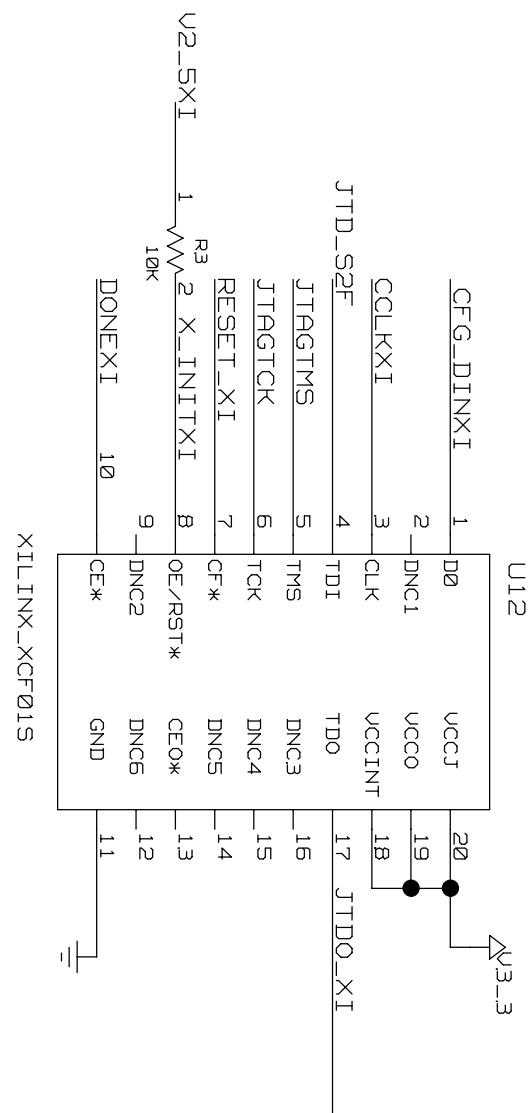
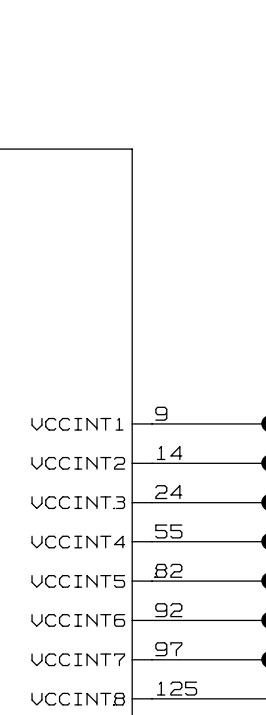
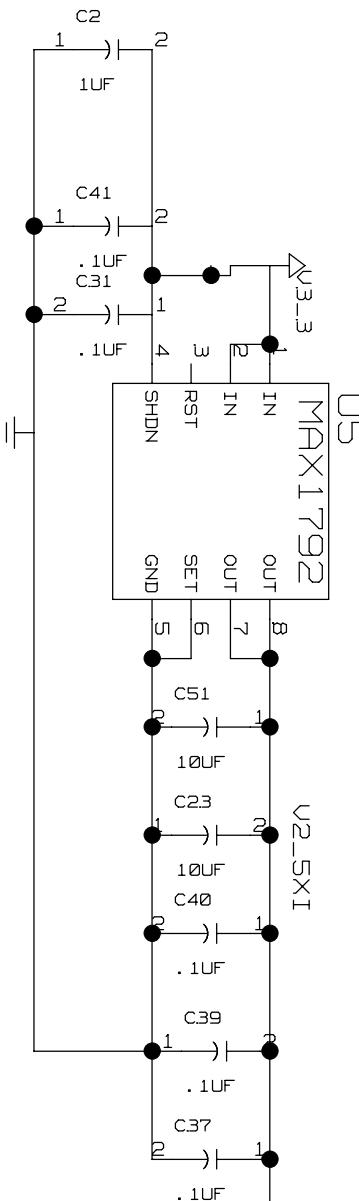
5 4

3

1

A B C D

TITLE:	DS26502DK01B0	DATE:	04/12/05
ENGINEER:	STEVE SCULLY	PAGE:	7 / 14



CLOCKS

TITLE:

DS26502DK01B0

DATE:

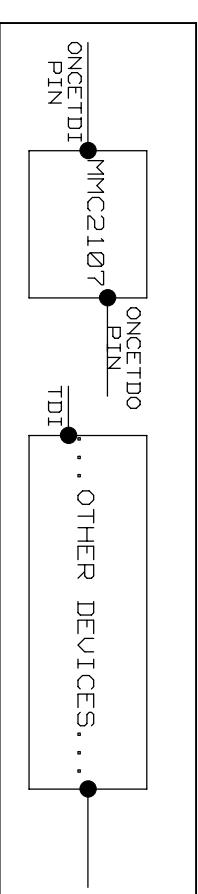
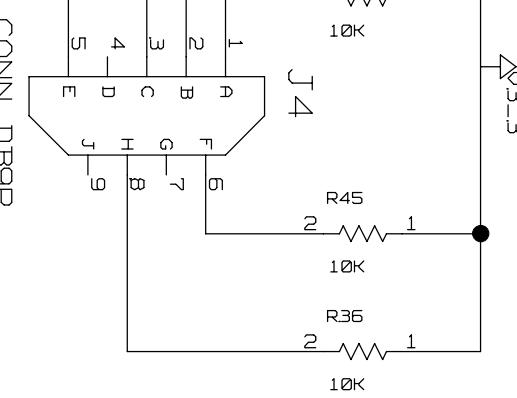
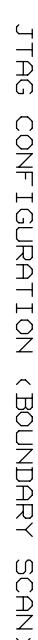
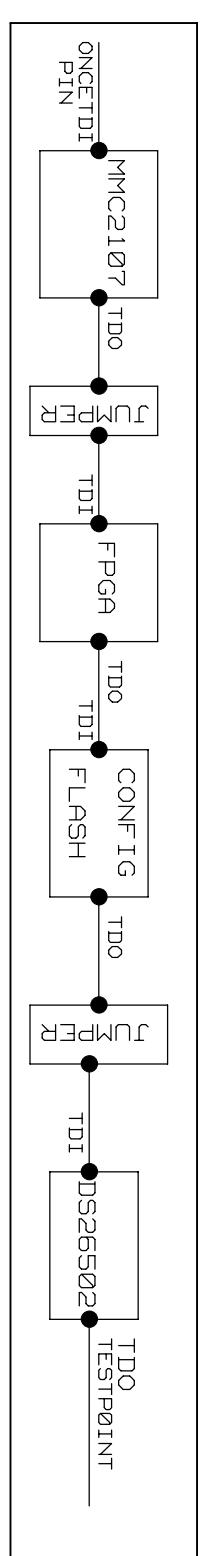
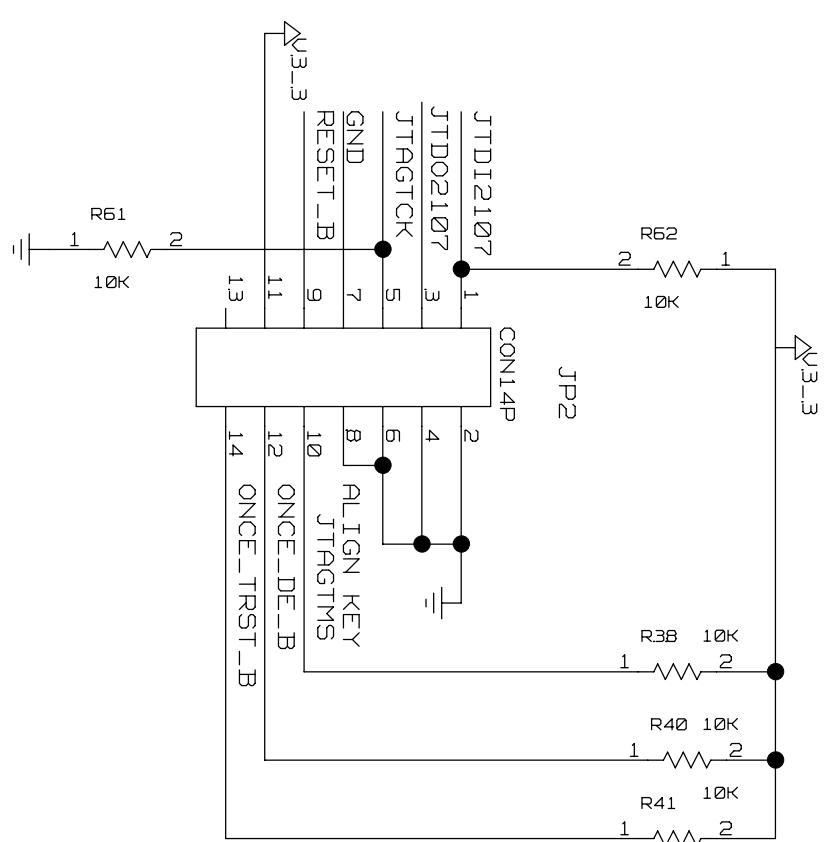
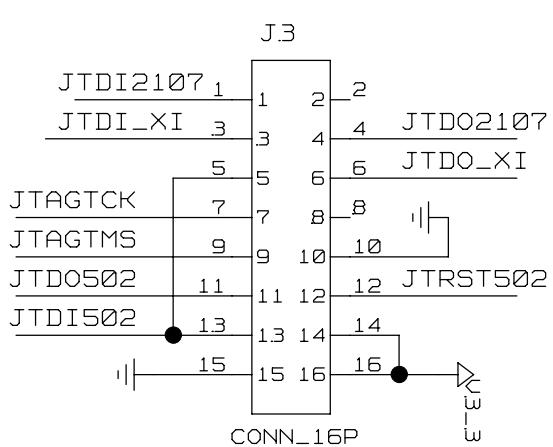
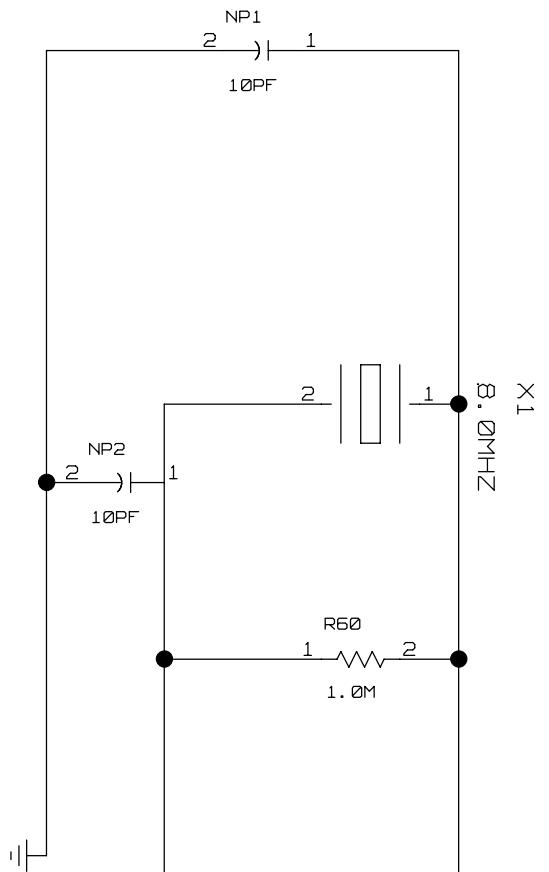
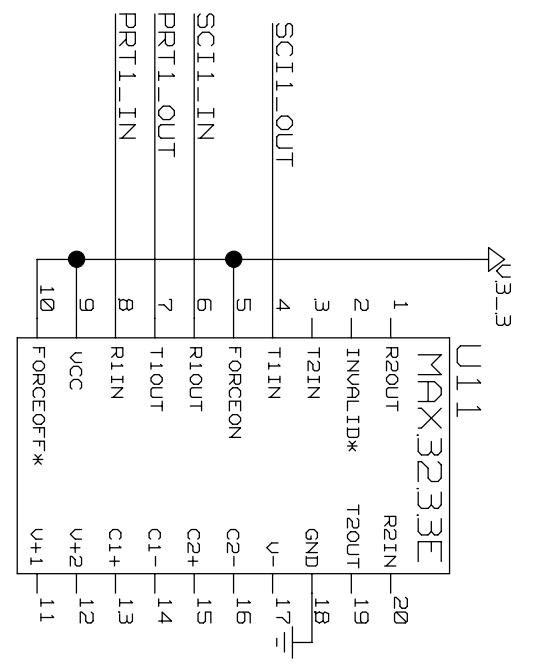
041205

ENGINEER:

STEVE SCULLY

PAGE:

B / 14



JTAG / ONCE  
DEBUG SELECTION

OSC\_MCU

CONN\_DB9P

1

2

81

10

3

४

၈

۷۶

B 7 6 5 4 3 2 1

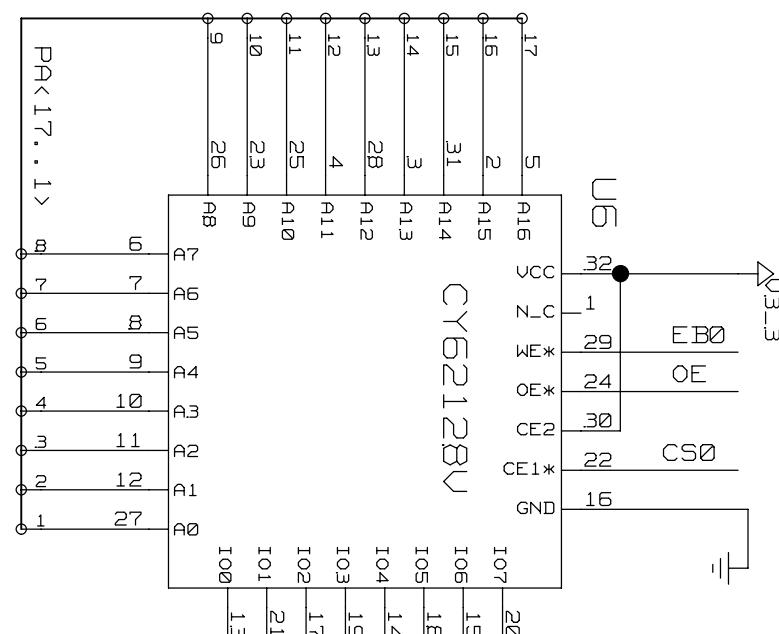
5

4

3

2

1

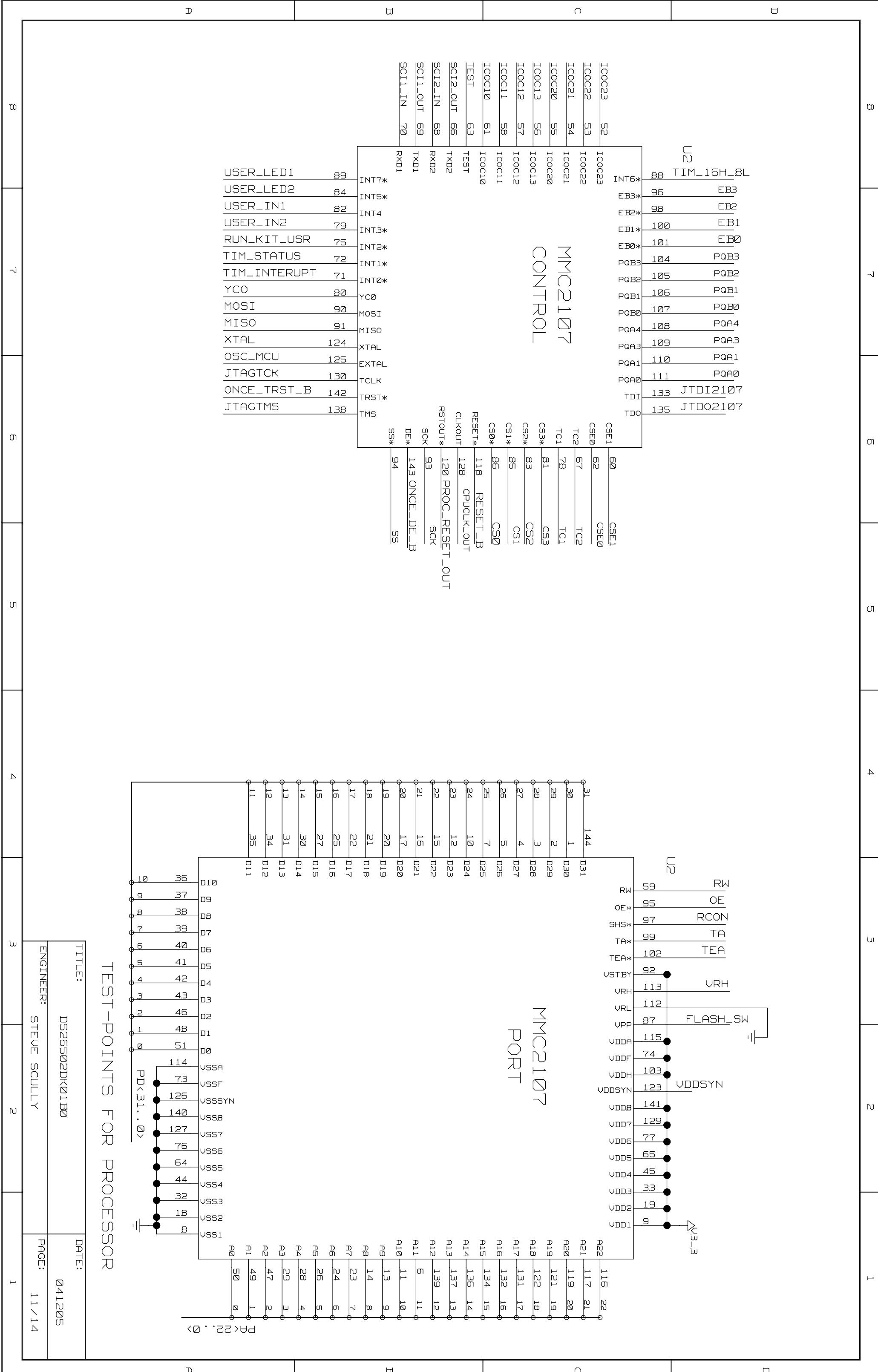


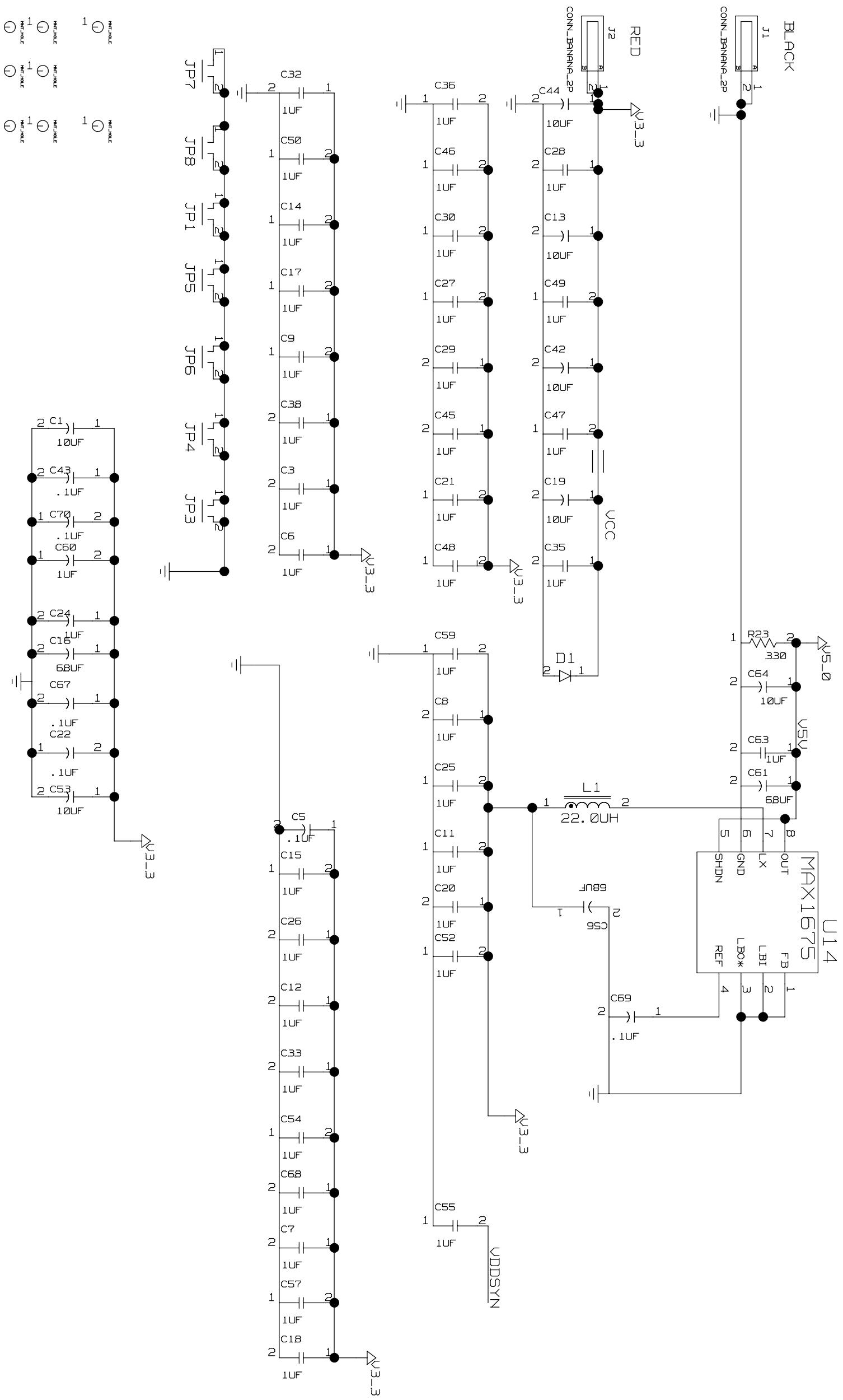
PD&lt;31..24&gt;

PD&lt;23..16&gt;

B	7	6	5	4	3	2	1
B	7	6	5	4	3	2	1

TITLE:	DS26502DK01B0	DATE:	041205
ENGINEER:	STEVE SCULLY	PAGE:	10 / 14





TITLE:	DS26502DK01B0
ENGINEER:	STEVE SCULLY
PAGE:	12 / 14

DATE:

041205

PAGE:

12 / 14

B 7 6 5 4 3 2 1

A		B		C		D	
RCLK502	RCON	5B<> 2C4<	6D3<> 11D3<> 7B<	4D5<> 5C2<	4A3<> 5B4<> 2B8<	6312..OSC	400HZ502
RD#502	RESET_XI	6B5<> 9C3<> 11B5<> 7A6<	7A7<> BART<> BC1<	2C4> 4C1 5D4<	2A1<> 4D6<>	ADDR#02<7..0>	B1S0#02
RL0F502	2B4> 5C7<> 5B<	2B4> 5C7<> 5B<	4A3<> 5B4<> 2CB<	4A2<> 5B4<>	7B5<	BT15#02	BOOT_SEL
RLOS502	2DB> 3B7<	2DB> 3B7<	4A2<> 5B4<>	4A2<> 5B4<>	4R2<	BT55#02	
RSER502	4B1<> 5B2<> 2C4<	4B1<> 5B2<> 2C8<	5B5<> 10D3<> 10D6<> 11A5<>	4B2<> BCI<	5B5<	CCLK_XTI	
RTIP502	4D6<> 5B8<> 2C8<	4D6<> 5B8<> 2C8<	6B5<> 11B5<> 4CB<	4B2<> BCI<	4R2<	CFG_DIN_XTI	
RUNKIT_USR	5A7<> 11A7<>	5A7<> 11A7<>	6C5<> 11C5<>	6C5<> 11C5<>	4A3<> 5B4<>	CPUCLK_OUT	CS#502
RW	4A5<> 6D3<> 11D3<>	4A5<> 6D3<> 11D3<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	CSE1	CS0
SC11_IN	6B8<> 9BB<> 11BB<>	6B8<> 9BB<> 11BB<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	DAT502<7..0>	DONE_XI
SCI1_OUT	6B8<> 11BB<> 9BB<	6B8<> 11BB<> 9BB<	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	E1..OSC	E1..OSC
SCI2_IN	6B8<> 11BB<>	6B8<> 11BB<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	EXT_OSC	EXT_OSC
SCI2_OUT	4A6<> 6B5<> 11BB<>	4A6<> 6B5<> 11BB<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	FLASH_SW	FLASH_SW
SCK	4A5<> 6B5<> 11BB<>	4A5<> 6B5<> 11BB<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	ICOC10	ICOC10
SS	4A5<> 6B5<> 11BB<>	4A5<> 6B5<> 11BB<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	ICOC11	ICOC11
T1..OSC	2D2<> 4D5<>	2D2<> 4D5<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	EB2	EB2
TA	4A6<> 6D3<> 11D3<>	4A6<> 6D3<> 11D3<>	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	TC1	TC1
TC2	4D6<> 5B2<> 2C8<	4D6<> 5B2<> 2C8<	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	TCLK502	TCLK502
TCLK502X1	4A3<> 2CB<	4A3<> 2CB<	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	TEST	TEST
TCLK0502	4D3<> 2CB<	4D3<> 2CB<	5C5<> 11C5<>	5C5<> 11C5<>	5C5<> 11C5<>	THZ502	THZ502
TCSS15#02	4B1> 6A7<> 7A4<> 11A7<>	4B1> 6A7<> 7A4<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	TEA	TEA
TMODE15#02	4D3<> 2CB<	4D3<> 2CB<	5B8<> 11B8<>	5B8<> 11B8<>	5B8<> 11B8<>	TMODE15#02	TMODE15#02
TMODE25#02	4D3<> 2CB<	4D3<> 2CB<	5B8<> 11B8<>	5B8<> 11B8<>	5B8<> 11B8<>	TNEG05#02	TNEG05#02
TPOS05#02	2C4> 5CB<>	2C4> 5CB<>	5B8<> 11B8<>	5B8<> 11B8<>	5B8<> 11B8<>	TRING5#02	TRING5#02
TSER5#02	4B1<> 2CB<	4B1<> 2CB<	5B8<> 11B8<>	5B8<> 11B8<>	5B8<> 11B8<>	TSTR5#02	TSTR5#02
TS_BK_45#02	5DB<> 2CB<	5DB<> 2CB<	5B8<> 11B8<>	5B8<> 11B8<>	5B8<> 11B8<>	TTIP5#02	TTIP5#02
TTIP5#02	4A3<> 2CB<	4A3<> 2CB<	5B8<> 11B8<>	5B8<> 11B8<>	5B8<> 11B8<>	JTD1..XTI	JTD1..XTI
USER_IN1	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	JTD02#02	JTD02#02
USER_IN2	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	5A7<> 7C3<> 11A7<>	JTD02#1#07	JTD02#1#07
USER_IN3	7C3<>	7C3<>	7C3<>	7C3<>	7C3<>	JTD02#1#07	JTD02#1#07
USER_IN4	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	JTD0..XI	JTD0..XI
USER_LLED1	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	JTD_S2#	JTD_S2#
USER_LLED2	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	5A7<> 11A7<> 7A4<	JTR5#02	JTR5#02
V2..5XI	7C3<>	7C3<>	7C3<>	7C3<>	7C3<>	MCLK5#02	MCLK5#02
USU	12D4<>	12D4<>	12D4<>	12D4<>	12D4<>	MCLK5#02X1	MCLK5#02X1
UDDSYN	6D2< 11D2< 12C1<	6D2< 11D2< 12C1<	6D3< 11D3<	6D3< 11D3<	6D3< 11D3<	M15#0	M15#0
URH	4A3<> 5B4<> 2CB<	4A3<> 5B4<> 2CB<	5B8<> 11B8<>	5B8<> 11B8<>	5B8<> 11B8<>	WR#502	WR#502
XTAL	5A6<> 9C5<> 11A7<>	5A6<> 9C5<> 11A7<>	5A6<> 9C5<> 11A7<>	5A6<> 9C5<> 11A7<>	5A6<> 9C5<> 11A7<>	X..INIT_XI	X..INIT_XI
YCO	4A2<> BART<>	4A2<> BART<>	5A7<> 11A7<>	5A7<> 11A7<>	5A7<> 11A7<>	ONCE..DE_B	ONCE..DE_B
Z..INIT_XI	4A2<> BART<>	4A2<> BART<>	5A7<> 11A7<>	5A7<> 11A7<>	5A7<> 11A7<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>
OSC..MCU	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	PAK15..0#	PAK15..0#
PAK22..0#	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	PAK15..0#	PAK15..0#
PAK17..1#	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	PD<31..0#	PD<31..0#
PD<23..16#	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	PD<31..15#	PD<31..15#
4FB#	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	5A6<> 9B2<> 11A5<>	PQ#4	PQ#4
PLL..CLK5#02	4D5<> 5C2<> 2C4<	4D5<> 5C2<> 2C4<	5C7<> 2CB< 4A3< 5C2<	5C7<> 2CB< 4A3< 5C2<	5C7<> 2CB< 4A3< 5C2<	PQB#0	PQB#0
PQA#0	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	PQB#1	PQB#1
PQA#1	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	PQB#2	PQB#2
PQA#3	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	5A6<> 11D7<>	PQB#3	PQB#3
PROC_RESET_OUT	4D5<> 5B5<> 11B5<>	4D5<> 5B5<> 11B5<>	5B8<> 9B2<> 9BB<	5B8<> 9B2<> 9BB<	5B8<> 9B2<> 9BB<	PRT1..IN	PRT1..IN
PRT1..OUT	9AB<> 9BB<	9AB<> 9BB<	9AB<> 9BB<	9AB<> 9BB<	9AB<> 9BB<	RA15#02	RA15#02

A B C D

A B C D

A B C D

A B C D

A B C D

A B C D

A B C D

A B C D

A B C D

A B C D

B

7

6

5

4

3

2

1

## \*\*\* Part Cross-Reference for the entire design \*\*\*

DSS	LED	4B1	R40	RES1	9C1
DS6	LED	5B7	R41	RES1	9C1
DS7	LED	5B7	R42	RES1	5B1
C1	CAP1	12B5	R43	RES1	7A3
C2	CAP1	B6B	R44	RES1	9A7
C3	CAP1	12B5	R45	RES1	9A7
C4	CAP1	3D5	R46	RES1	5B1
C5	CAP1	12B3	R47	RES1	7A3
C6	CAP1	12B5	R48	RES1	2C7
C7	CAP1	12B1	R49	RES1	5B1
C8	CAP1	12B4	R50	RES1	7B3
C9	CAP1	12B5	R51	RES1	2C4
C10	CAP1	5DB	R52	RES1	3A5
C11	CAP1	12B3	R53	RES1	7D7
C12	CAP1	12B2	R54	RES1	2C4
C13	CAP1	12B6	R55	RES1	2C8
C14	CAP1	12B5	R56	RES1	5C1
C15	CAP1	12B3	R57	RES1	2C5
C16	CAP1	12B4	R58	RES1	7A3
C17	CAP1	12B6	R59	RES1	5C1
C18	CAP1	12B1	R60	RES1	9D5
C19	CAP1	12B5	R61	RES1	9B2
C20	CAP1	12B3	R62	RES1	2A2
C21	CAP1	12B5	R63	RES1	4D2
C22	CAP1	12B4	R64	RES1	4D2
C23	CAP1	B6G	R65	RES1	5C1
C24	CAP1	12B4	R66	RES1	2A2
C25	CAP1	12B3	R67	RES1	7A3
C26	CAP1	12B6	R68	RES1	4D2
C27	CAP1	12B5	R69	RES1	5B7
C28	CAP1	12B6	R70	RES1	5B7
C29	CAP1	12B5	R71	RES1	2A2
C30	CAP1	12B3	R72	RES1	7A3
C31	CAP1	B6B	R73	RES1	7A3
C32	CAP1	12B7	R74	RES1	7A3
C33	CAP1	12B2	R75	RES1	7A3
C34	CAP1	3A6	R76	RES1	7A3
C35	CAP1	12B4	R77	RES1	7A3
C36	CAP1	12B6	R78	RES1	7A3
C37	CAP1	12B7	R79	RES1	7A3
C38	CAP1	12B2	R80	RES1	7A3
C39	CAP1	BC6	R81	RES1	7A3
C40	CAP1	12B4	R82	RES1	7A3
C41	CAP1	12B6	R83	RES1	7A3
C42	CAP1	12B7	R84	RES1	7A3
C43	CAP1	12B5	R85	RES1	7A3
C44	CAP1	12C7	R86	RES1	7A3
C45	CAP1	12B5	R87	RES1	7A3
C46	CAP1	BC6	R88	RES1	7A3
C47	CAP1	12B5	R89	RES1	7A3
C48	CAP1	12B4	R90	RES1	7A3
C49	CAP1	12B6	R91	RES1	7A3
C50	CAP1	12B5	R92	RES1	7A3
C51	CAP1	BC7	R93	RES1	7A3
C52	CAP1	12B6	R94	RES1	7A3
C53	CAP1	12B3	R95	RES1	7A3
C54	CAP1	12B6	R96	RES1	7A3
C55	CAP1	12B5	R97	RES1	7A3
C56	CAP1	12C3	R98	RES1	7A3
C57	CAP1	12B3	R99	RES1	7A3
C58	CAP1	12B4	R100	RES1	7A3
C59	CAP1	12B2	R101	RES1	7A3
C60	CAP1	12B4	R102	RES1	7A3
C61	CAP1	12B3	R103	RES1	7A3
C62	CAP1	12B2	R104	RES1	7A3
C63	CAP1	12B4	R105	RES1	7A3
C64	CAP1	12B4	R106	RES1	7A3
C65	CAP1	2D3	R107	RES1	7A3
C66	CAP1	12B3	R108	RES1	7A3
C67	CAP1	12B4	R109	RES1	7A3
C68	CAP1	12B2	R110	RES1	7A3
C69	CAP1	12B2	R111	RES1	7A3
C70	CAP1	12B5	R112	RES1	7A3
D1	DIODE	12C4	R113	RES1	7A3
D2	LED	7A3	R114	RES1	9C1
DS2	LED	7B3	R115	RES1	5B1
DS3	LED	7B3	R116	RES1	5B1
DS4	LED	7D1	R117	RES1	5B1

## REVISION HISTORY:

041205 - INITIAL RELEASE OF 01B0 VERSION.  
 THIS VERSION IS EXACTLY LIKE THE 01A0  
 VERSION EXCEPT FOR THE FOLLOWING:  
 - SIGNAL RCLK502 WAS CONNECTED TO THE  
 FPGA, U4, AT PIN 63.  
 - THE PINS WERE SNAPPED ON C13, C42 & C61

A			B		C
DSS	LED	4B1	R40	RES1	9C1
DS6	LED	5B7	R41	RES1	9C1
DS7	LED	5B7	R42	RES1	5B1
DS8	LED	7B3	R43	RES1	7A3
DS10	LED	7B3	R44	RES1	9A7
J1	CONN_BANANA_2P	12D7	R45	RES1	9A7
J2	CONN_BANANA_2P	12C7	R46	RES1	5B1
J3	CONN_16P	9B5	R47	RES1	7A3
J4	CONN_DB9_9P	9A7	R48	RES1	2C7
J5	CONN_BNC_5P	4D1	R49	RES1	5B1
J6	CONN_16P	5B3	R50	RES1	7B3
J7	CONN_16P	5D3	R51	RES1	2C4
J8	CONN_BANTAM_1PC	3C2	R52	RES1	2C5
J9	CONN_RJ45_3P4	3B4	R53	RES1	2C4
J10	CONN_BNC_5P	3D3	R54	RES1	2C4
J11	CONN_BNC_5P	3A4	R55	RES1	2C8
J12	CONN_BANTAM_3B2	3B2	R56	RES1	5C1
J13	CONN_BANTAM_3B2	3B2	R57	RES1	9B2
J14	CONN_16P	4D1	R58	RES1	2A2
J15	CONN_BNC_5P	3D3	R59	RES1	4D2
J16	CONN_16P	4D1	R60	RES1	9D5
J17	CONN_16P	4D1	R61	RES1	2A2
J18	CONN_16P	4D1	R62	RES1	7A3
J19	CONN_16P	4D1	R63	RES1	4D2
J20	CONN_16P	4D1	R64	RES1	4D2
J21	CONN_16P	4D1	R65	RES1	5C1
J22	CONN_16P	4D1	R66	RES1	2A2
J23	CONN_16P	4D1	R67	RES1	7A3
J24	CONN_16P	4D1	R68	RES1	7A3
J25	CONN_16P	4D1	R69	RES1	7A3
J26	CONN_16P	4D1	R70	RES1	7A3
J27	CONN_16P	4D1	R71	RES1	2A2
J28	CONN_16P	4D1	R72	RES1	7A3
J29	CONN_16P	4D1	R73	RES1	7A3
J30	CONN_16P	4D1	R74	RES1	7A3
J31	CONN_16P	4D1	R75	RES1	7A3
J32	CONN_16P	4D1	R76	RES1	7A3
J33	CONN_16P	4D1	R77	RES1	7A3
J34	CONN_16P	4D1	R78	RES1	7A3
J35	CONN_16P	4D1	R79	RES1	7A3
J36	CONN_16P	4D1	R80	RES1	7A3
J37	CONN_16P	4D1	R81	RES1	7A3
J38	CONN_16P	4D1	R82	RES1	7A3
J39	CONN_16P	4D1	R83	RES1	7A3
J40	CONN_16P	4D1	R84	RES1	7A3
J41	CONN_16P	4D1	R85	RES1	7A3
J42	CONN_16P	4D1	R86	RES1	7A3
J43	CONN_16P	4D1	R87	RES1	7A3
J44	CONN_16P	4D1	R88	RES1	7A3
J45	CONN_16P	4D1	R89	RES1	7A3
J46	CONN_16P	4D1	R90	RES1	7A3
J47	CONN_16P	4D1	R91	RES1	7A3
J48	CONN_16P	4D1	R92	RES1	7A3
J49	CONN_16P	4D1	R93	RES1	7A3
J50	CONN_16P	4D1	R94	RES1	7A3
J51	CONN_16P	4D1	R95	RES1	7A3
J52	CONN_16P	4D1	R96	RES1	7A3
J53	CONN_16P	4D1	R97	RES1	7A3
J54	CONN_				