

Low drop adjustable positive voltage regulator





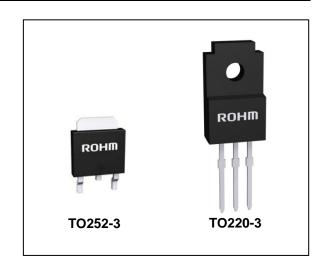
BA1117FP

Features

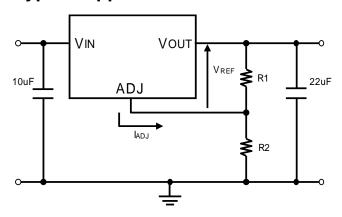
- Low dropout voltage:
 - 1.2 V typ. (at $Io = 1 A, 25^{\circ}C$)
- Output current up to 1 A
- Adjustable version availability (VREF = 1.25 V)
- Internal current and thermal limit
- Available in ±1% (at 25°C) and 2% in full temperature range
- High supply voltage rejection:
 - 75 dB typ. (at 25°C)
- Temperature range: -20°C to 105°C
- Designed to use by ceramic capacitors



The BA1117FP is a low drop voltage regulator able to provide up to 1 A of output current, available in adjustable versions (VREF =1.25V). The device is supplied in: TO252-3 and TO220-3. Surface mounted packages optimize the thermal characteristics while offering a relevant space saving advantage. High efficiency is assured by NPN pass transistor. Only a very common 22uF minimum capacitor is needed for stability. Chip trimming allows the regulator to reach a very tight reference voltage tolerance, within $\pm 1\%$ at 25°C .



Typical Application



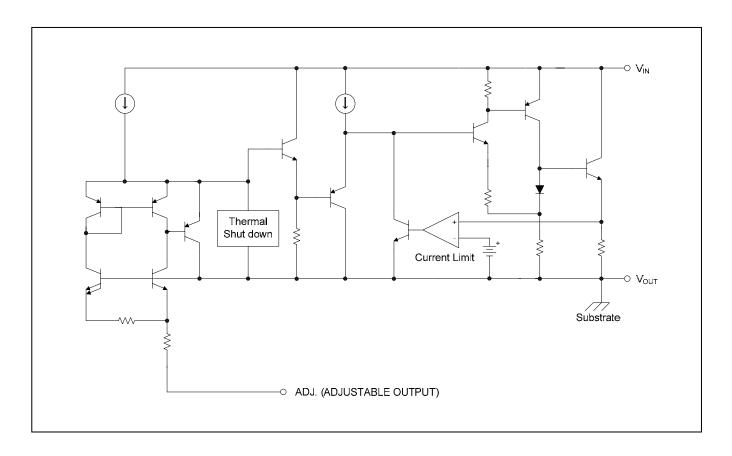
VREF = 1.25 V (Typ.) IADJ = 60 uA (Typ.) $VO = VREF \times (1 + R_2 / R_1) + IADJ \times R_2$

Table1. Device summary

Order	codes	Quitnut voltage	
TO252-3	TO220-3	Output voltage	
BA1117FP-E2	Under development	Adjustable from 1.25 V	

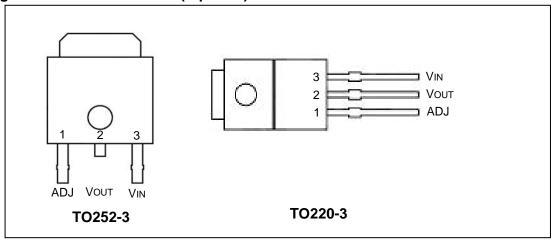
● Diagram

Figure 1. Block diagram



●Pin configuration

Figure 2. Pin connections (top view)



Note1: The TAB is connected to the Vout.

Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VIN DC input voltage		15	V
Pb	PD Power dissipation		W
TSTG Storage temperature range		-55 to +150	°C
Top Operating junction temperature range		-20 to +105	°C

Note2: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied. Beyond the above suggested max. power dissipation, a short-circuit may permanently damage the device.

Note3: In case $Ta \ge 25 \,^{\circ}C(70 \text{mm} \times 70 \text{mm} \times 1.6 \text{mm} \text{ when mounted on a glass epoxy board)}$ is reduced by $9.6 \text{mW}/^{\circ}C$.

Table 3. Thermal data

Symbol	Parameter	TO252-3	TO220-3	Unit
RthJA	Thermal resistance junction-ambient	104.2	67.5	°C/W

Electrical characteristics

Refer to the test circuits, $T_J = -20$ to 105° C, $C_O = 22$ uF, $C_I = 10$ uF, unless otherwise specified.

Table 4. Electrical characteristics of BA1117 (Adjustable)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
		VI = 5.3 V, IO = 10 mA, TJ = 25°C	1.238	1.250	1.262	V
		Io = 10 mA to 1 A, VI = 2.75 to 10 V	1.225		1.27	V
⊿Vo	Line regulation	VI = 2.75 V to 8 V, Io = 0 mA		1	6	mV
⊿Vo	Load regulation	VI = 2.75 V, IO = 0 to 1A		1	10	mV
⊿Vo	Temperature stability			0.5		%
⊿Vo	Long term stability	1000hrs, T _J = 105°C		0.3		%
Vı	Operating input voltage	Io = 100mA			10	V
IADJ	Adjustment Pin Current	Vi ≦ 10 V		60	120	uA
⊿IADJ	Adjustment Pin Current Change	VI - Vo =1.4 to 10 V, Io = 10 mA to 1 A		0.2	5	uA
IO(min)	Minimum Load Current	VI = 10 V		1.7	5	mA
lo	Output current	Vı - Vo = 5 V, Tı = 25°C	1000	1700		mA
eN	Output noise voltage B = 10 Hz to 10 kHz, TJ = 25°C			100		uV
SVR	Supply voltage rejection	Io = 40mA, f = 120 Hz VI - VO = 3 V, Vripple = 1 VPP,	60	75		dB
		Io = 100 mA		1	1.10	V
VD	Dropout voltage	Io = 500 mA		1.05	1.15	V
		Io = 1 A		1.20	1.40	V
∠VO(pwr)	Thermal regulation	Ta = 25°C, 30 ms pulse		0.08	0.2	%/W

Electrical characteristics (reference data)

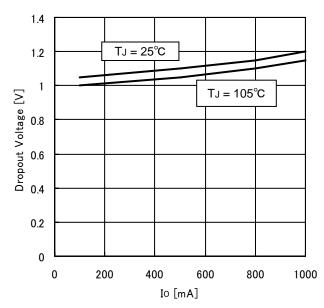


Figure 3. Dropout voltage

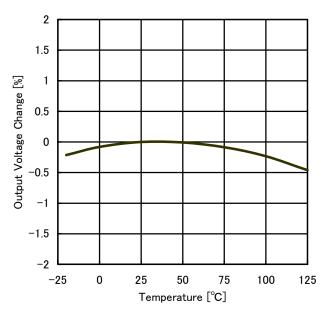


Figure 4. Temperature Stability

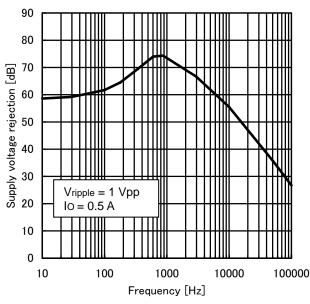


Figure 5. Supply voltage rejection

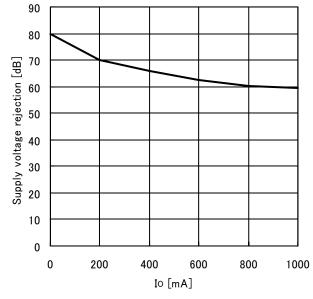


Figure 6. Supply voltage rejection vs lo

Electrical characteristics (reference data)

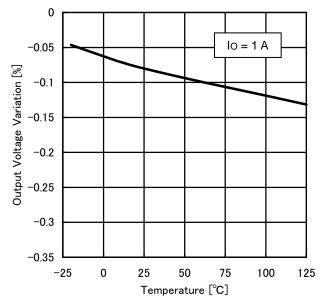


Figure 7. Load regulation

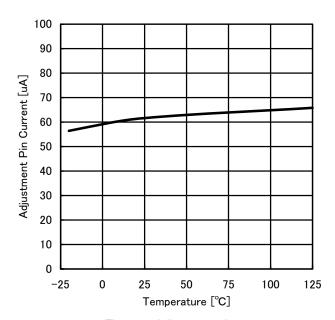


Figure 8. Adjustment pin current

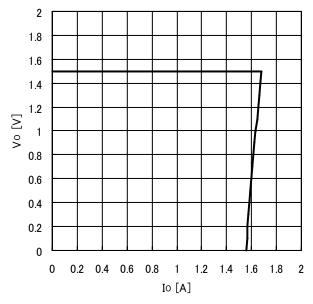


Figure 9. Load regulation vs Vo

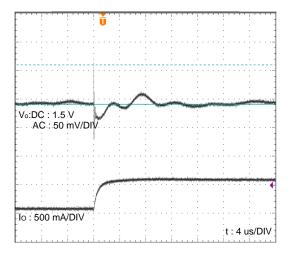


Figure 10. Load Transient Response (0→0.5A) Co=22µF

●BA1117 adjustable: application note

The BA1117 adjustable has a thermal stabilized 1.25 \pm 0.012V reference voltage between the Vout and ADJ pins. IADJ is 60uA typ. (120uA max.) and \triangle IADJ is 0.2uA typ(5uA max.). R₁ is normally fixed to 120 Ω .

 $VO = VREF + R_2 (IADJ + IR_1) = VREF + R_2 (IADJ + VREF / R_1) = VREF (1 + R_2 / R_1) + R_2 \times IADJ.$

In normal applications the R_2 value is in the range of a few $k\Omega$, so the $R_2 \times I_{ADJ}$ product can not be considered in the Vo calculation; the above expression then becomes:

 $Vo = VREF (1 + R_2 / R_1).$

In order to have a better load regulation it is important to realize a good Kelvin connection of R₁ and R₂ resistors. In particular, the R₁ connection must be realized very close to the Vout and ADJ pins, while the R₂ ground connection must be placed as near as possible to the negative load pin. Ripple rejection can be improved by introducing a 10uF electrolytic capacitor placed in parallel to the R₂ resistor (see Figure 11, 12).

The output capacitor is critical in maintaining regulator stability, and must meet the required conditions for both minimum amount of capacitance and ESR(Equivalent Series Resistance). The minimum output capacitance required by the BA1117FP is 22uF, if a ceramic/tantalum capacitor is used. Any increase of the output capacitance will merely improve the loop stability and transient response. The ESR of the output tantalum capacitor should range between $0.3\,\Omega$ - $5\,\Omega$.

Figure. 11 Adjustable output voltage application

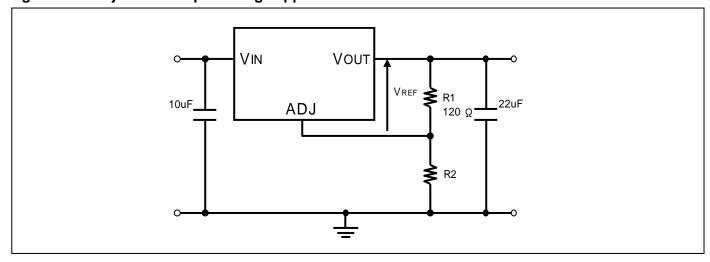
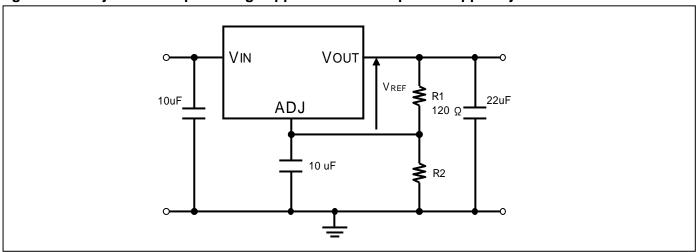


Figure. 12 Adjustable output voltage application with improved ripple rejection

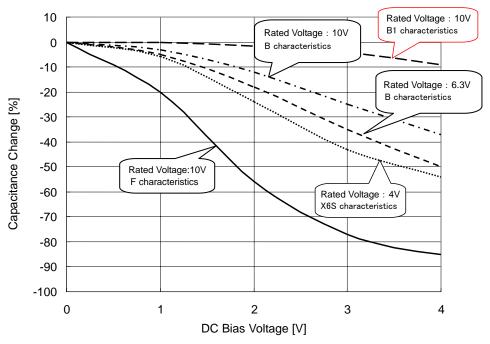


●Input- to-Output Capacitor

It is recommended that a capacitor is placed very close between Input pin and GND, output pin and GND.

A capacitor, between input pin and GND, is valid when the power supply impedance is high or the trace is long. Also as for a capacitor, between output pin and GND, the greater the capacity, more sustainable the line regulation and it makes improvement of the characteristics depending on the load. However, please check the actual functionality of this part by mounting on a board for the actual application. Ceramic capacitor usually have different, thermal and equivalent series characteristics, and moreover capacitance decreases gradually in use.

For additional detail, please check the manufacturer, and select the best ceramic capacitor for your application.



Ceramic capacitor capacity – DC bias characteristics (Characteristics example)

Operatinal Notes

(1). Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify damage mode, such as a short circuit or an open circuit. If there is any possibility of exposure over the rated values, please consider adding circuit protection devices, such as fuses.

(2). Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3). Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When using electrolytic capacitors in the circuit, note that capacitance values are reduced at low temperatures and over time.

(4). GND voltage

The potential of GND pin must be minimum potential under all operating conditions.

(5). Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6). Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

(7). Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as this may cause the IC to malfunction.

(8). ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(9). Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

(10). Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply before connecting it or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

(11). Regarding input pin of the IC

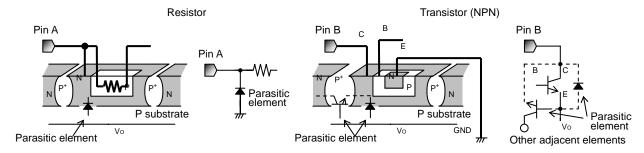
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated.P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When Vo > Pin A and Vo > Pin B, the P-N junction operates as a parasitic diode.

When Vo > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC.

The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the Vo (P substrate) voltage to an input pin, should not be used.

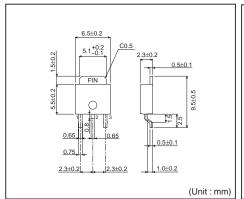


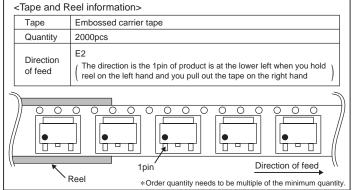
(12). Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

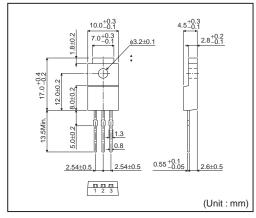
Physical Dimension/Tape and Reel Information

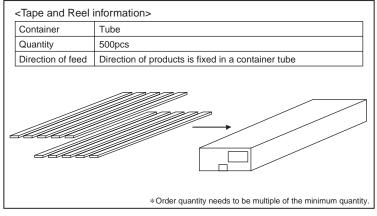
TO252-3



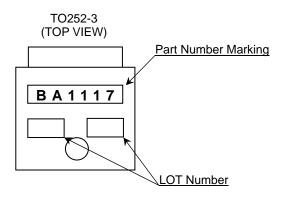


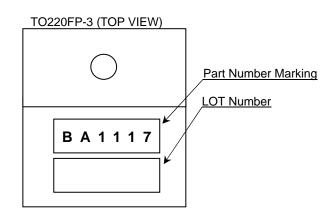
TO220FP-3





Marking Diagram





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