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# FDS2672\_F085

## N-Channel UltraFET Trench® MOSFET

200V, 3.9A, 70mΩ

### Features

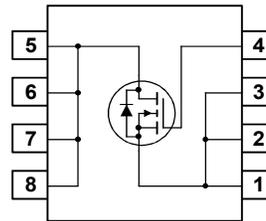
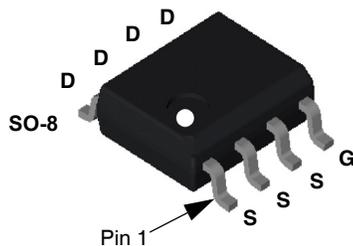
- Max  $r_{DS(on)}$  = 70mΩ at  $V_{GS} = 10V$ ,  $I_D = 3.9A$
- Max  $r_{DS(on)}$  = 80mΩ at  $V_{GS} = 6V$ ,  $I_D = 3.5A$
- Fast switching speed
- High performance trench technology for extremely low  $r_{DS(on)}$
- Qualified to AEC Q101
- RoHS compliant

### General Description

This single N-Channel MOSFET is produced using Fairchild Semiconductor's advanced UltraFET Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC-DC conversion



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	200	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Note 1a)	3.9	A
	-Pulsed	50	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	37.5	mJ
$P_D$	Power Dissipation (Note 1a)	2.5	W
	Power Dissipation (Note 1b)	1.0	
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	125	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS2672	FDS2672_F085	13"	12mm	2500 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	200			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		206		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 160\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
		$V_{DS} = 160\text{V}, V_{GS} = 0\text{V}$ $T_J = 55^\circ\text{C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA

**On Characteristics (Note 2)**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-11		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 3.9\text{A}$		59	70	m $\Omega$
		$V_{GS} = 6\text{V}, I_D = 3.5\text{A}$		63	80	
		$V_{GS} = 10\text{V}, I_D = 3.9\text{A}, T_J = 125^\circ\text{C}$		124	148	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 3.9\text{A}$		15		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1905	2535	pF
$C_{oss}$	Output Capacitance			100	135	pF
$C_{rss}$	Reverse Transfer Capacitance			30	45	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$		0.7	

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{V}, I_D = 3.9\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		22	35	ns
$t_r$	Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			35	56	ns
$t_f$	Fall Time			10	20	ns
$Q_g(TOT)$	Total Gate Charge at 10V			33	46	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 100\text{V}, I_D = 3.9\text{A}$		11		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$V_{GS} = 0\text{V}, I_S = 3.9\text{A}$		0.75	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 3.9\text{A}, di/dt = 100\text{A}/\mu\text{s}$		67	101	ns
$Q_{rr}$	Reverse Recovery Charge	$I_F = 3.9\text{A}, di/dt = 100\text{A}/\mu\text{s}$		179	269	nC

**Notes:**

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



Scale 1:1 on letter size paper

a)  $50^\circ\text{C}/\text{W}$  (10 sec)  
 $62.5^\circ\text{C}/\text{W}$  steady state  
when mounted on a  $1\text{in}^2$   
pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a  
minimum pad.

2: Pulse Test: Pulse Width < 300 us, Duty Cycle < 2.0%.  
3: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 5\text{A}$ ,  $V_{DD} = 100\text{V}$ ,  $V_{GS} = 10\text{V}$

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

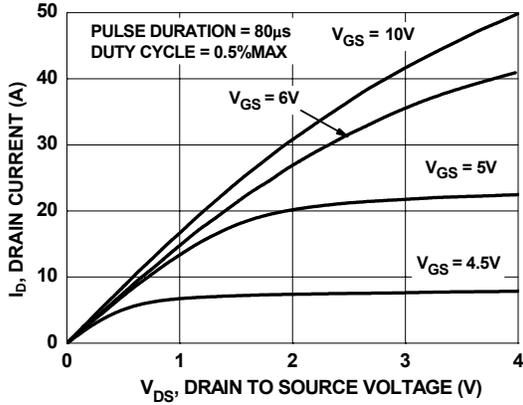


Figure 1. On Region Characteristics

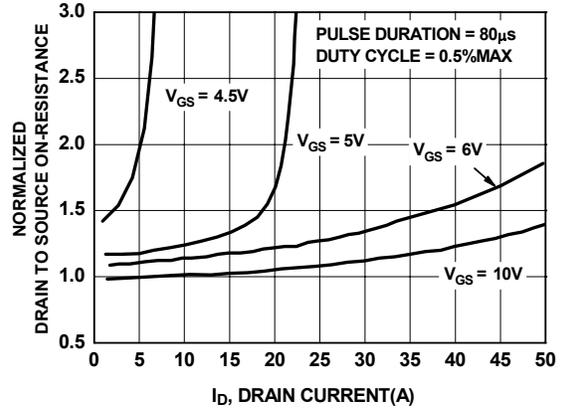


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

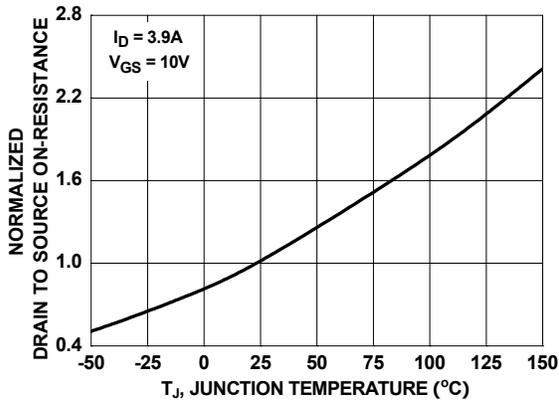


Figure 3. Normalized On Resistance vs Junction Temperature

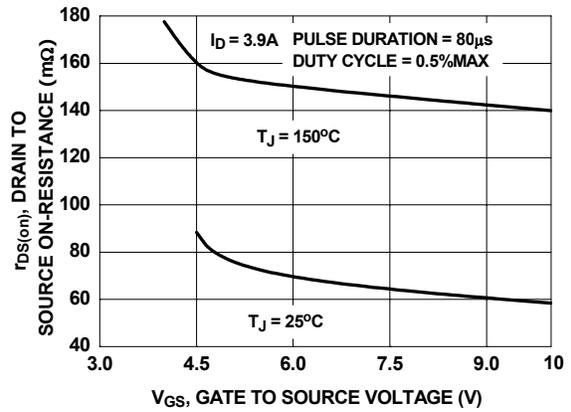


Figure 4. On-Resistance vs Gate to Source Voltage

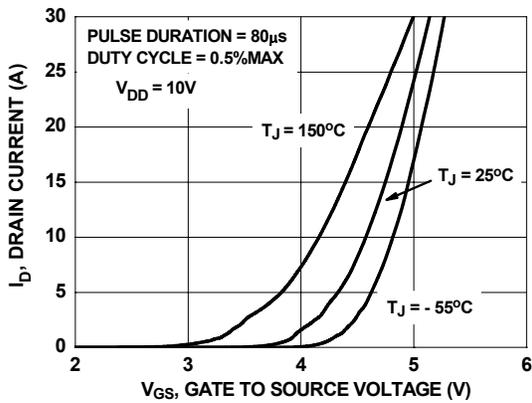


Figure 5. Transfer Characteristics

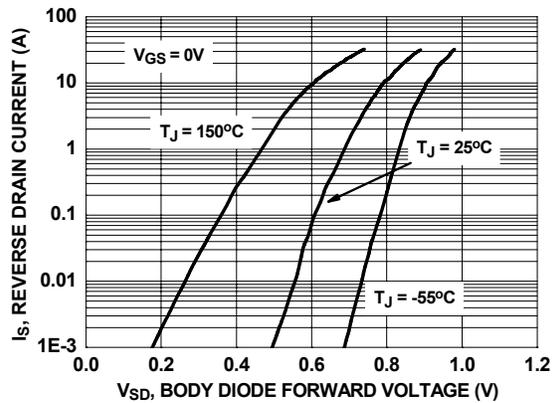


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

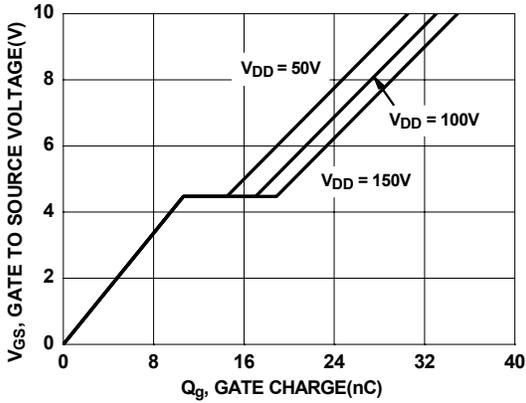


Figure 7. Gate Charge Characteristics

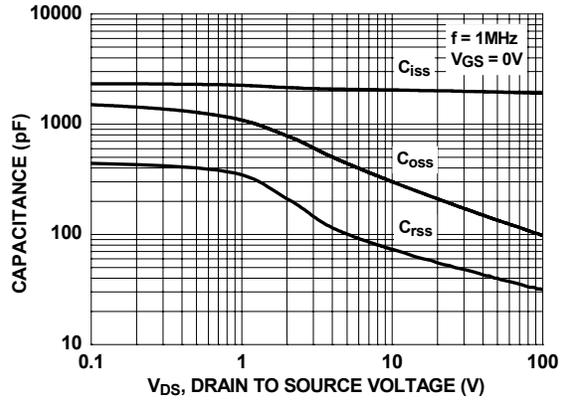


Figure 8. Capacitance vs Drain to Source Voltage

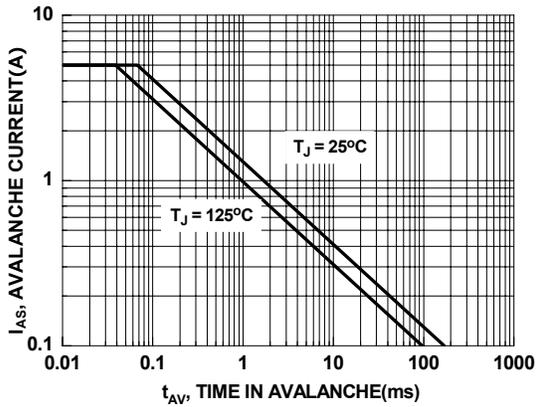


Figure 9. Unclamped Inductive Switching Capability

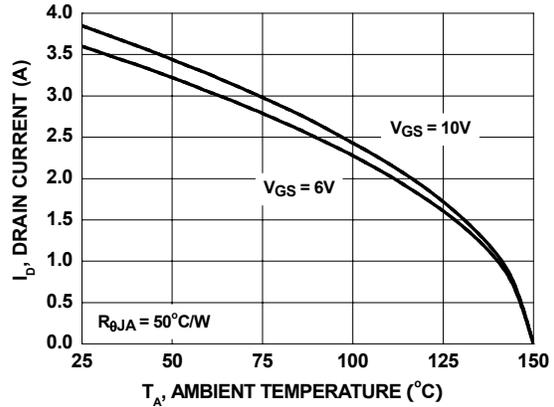


Figure 10. Ambient Continuous Drain Current vs Case Temperature

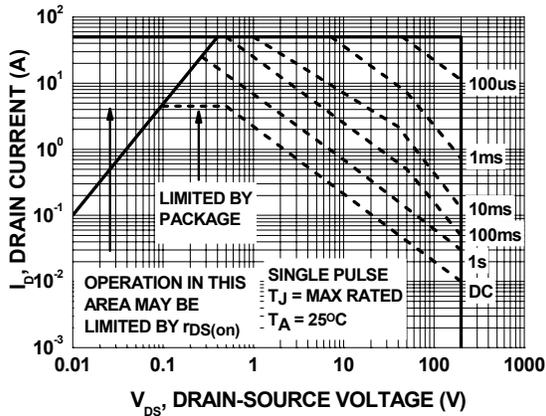


Figure 11. Forward Bias Safe Operating Area

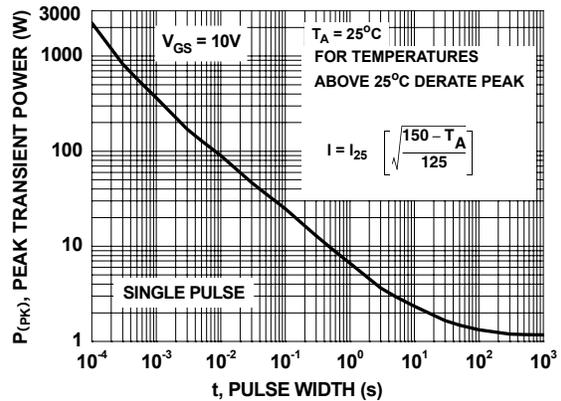
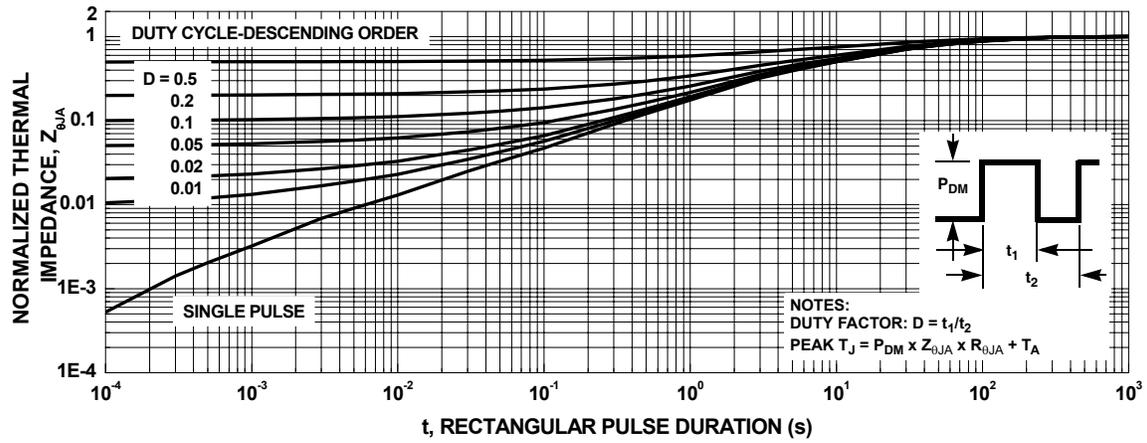


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted





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