

General Description

The MAX4887 triple, high-frequency switch is intended for notebooks and monitors to permit RGB signals to be switched from one driver to one of two loads (1:2) or one of two sources to be connected to one load (2:1). The MAX4887 high-performance switch utilizes n-channel architecture with internal high-drive pullup from a lownoise charge pump, resulting in very low on-capacitance.

The MAX4887 features 5Ω (typ) on-resistance switches with 10pF on-capacitances for routing RGB video signals. A logic input enables or disables the internal charge pump for optimal frequency performances when operating at lower input voltages resulting in standby supply current less than 3µA. All RGB inputs/outputs are ESD protected to ±8kV Human Body Model (HBM) and feature a global input (EN) that places all inputs and outputs in a high-impedance state.

The MAX4887 is available in a small 3mm x 3mm, 16pin TQFN package for ease of assembly and flowthrough layout, resulting in minimum space requirement and simplicity in board layout. The MAX4887 operates over the -40°C to +85°C temperature range.

Applications

Notebook Computers Servers and Routers **Docking Stations** PC/HDTV Monitors

Features

- ♦ +3V/+5V Single-Supply Operation
- ♦ Low Ron $5\Omega (V+=5V)$
- ♦ Low 10pF (typ) Con
- ♦ Global ENABLE Input to Turn On/Off Switches
- ♦ Break-Before-Make Switching
- ♦ ±8kV HBM ESD Protection per IEC1000-4-2 on I/Os
- ♦ Less than 1mA Supply Current (Charge Pump **Enabled**)
- ♦ Less than 3µA Standby Mode
- ♦ Charge-Pump Noise Lower than 163µVp-p
- ♦ Flowthrough Layout for Easy Board Layout
- ♦ Space-Saving Lead-Free (3mm x 3mm) 16-Pin **TQFN Package**

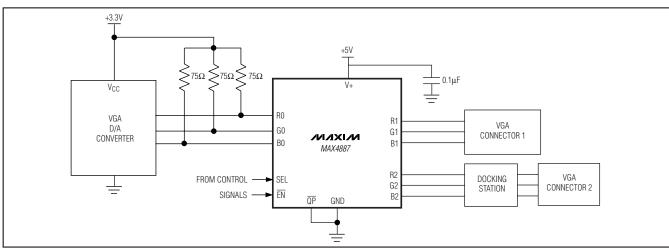
Ordering Information

PART	TEMP	PIN-	TOP	PKG
	RANGE	PACKAGE	MARK	CODE
MAX4887ETE	-40°C to +85°C	16 TQFN-EP* 3mm x 3mm	AEF	T1633-4

^{*}EP = Exposed paddle.

The MAX4887 is available only in a lead-free package. Specify lead-free by adding the + symbol at the end of the part number when ordering.

Typical Operating Circuit



NIXIN

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+0.3V to +6V
R_{-} , G_{-} , B_{-} , SEL , \overline{QP} , \overline{EN} (Note 1)0.3V to (V+ + 0.3V)
Continuous Current through Any Switch±120mA
Peak Current through Any Switch
(pulsed at 1ms, 10% duty cycle)±240mA

Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
16-Pin Thin QFN-EP (derate 15.6mW/°C above	
+70°C)	1250mW
Operating Temperature Range	40°C to +85°C
Storage Temperature Range68	5°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—5V SUPPLY

 $(V+=5V,\overline{QP}=GND,\,T_A=T_{MIN}\,to\,T_{MAX}.\,Typical\,\,values\,\,are\,\,at\,\,T_A=+25^{\circ}C,\,unless\,\,otherwise\,\,noted.)\,\,(Note\,\,2)$

PARAMETER	SYMBOL	CONDIT	IONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage Range				4.5		5.5	V
Quiescent Supply Current		V+ = +5.5V	$\overline{QP} = GND$		0.5	1	mA
Quiescent Supply Current	I ₊	V+ = +5.5V	$\overline{QP} = V +$		1	3	μΑ
RGB SWITCHES							
On-Resistance	Ron	$V_{IN} = +1.5V,$	$\overline{QP} = GND$		5	6.5	Ω
On-nesistance	HON	$I_{IN} = -25mA$	$\overline{QP} = V +$		6	7.5	22
On-Resistance Matching	ΔR _{ON}	$0.3V < V_{IN} < +2V$	$\overline{QP} = GND$		0.5	1.3	Ω
On-nesistance Matching	ΔhON	I _{IN} = -25mA (Note 3)	$\overline{QP} = V +$		0.7	1.5	52
		$0 < V_{IN} < +2V,$	$\overline{QP} = GND$		0.5	1	
On-Resistance Flatness	D=: +=(0.1)	$I_{IN} = -25 \text{mA}$	$\overline{QP} = V +$		0.7	1.8	Ω
On-nesistance riathess	RFLAT(ON)	$0 < V_{IN} < +1.5V, I_{IN} = -25mA$	QP =V+		0.7	1.55	22
On-Leakage Current	I _L (ON)	R_, G_, B_ = 0.7V, 4.8V;	EN = GND	-1		+1	μA
Off-Leakage Current	I _L (OFF)	R_, G_, B_ = 0.7V, 4.8V;	EN = GND		300		рΑ
LOGIC INPUTS (SEL, EN, QP)				•			
land Law Vallage	1/	V+ = 4.5V				0.8	V
Input Low Voltage	VIL	V+ = 5.5V				0.8	V
Innest High Valtage	\/	V+ = 4.5V		2.0			V
Input High Voltage	VIH	V+ = 5.5V		2.0			V
Input Leakage Current	ILEAK			-1		+1	μΑ
ESD PROTECTION							
CCD Protection		Human Body Model, R_,	G_, B_		±8		14/7
ESD Protection		Human Body Model, SE	L, EN, QP		±2		kV

AC ELECTRICAL CHARACTERISTICS—5V SUPPLY

 $(V+ = +5V, \overline{QP} = GND, T_A = T_{MIN} \text{ to } T_{MAX}. \text{ Typical values are at } T_A = +25^{\circ}C, \text{ unless otherwise noted.})$ (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charge-Pump Noise	VQP	$R_S = R_L = 50\Omega$			163		μV _{P-P}
Turn-On Time	ton	V_{IN} = +4.5V, R_L = 100 Ω , Figure	2			20	μs
Charge Injection		$V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, $C_L = 1.0$	nF, Figure 3		28		рС
Propagation Delay	tplh/tphl	$C_L = 10$ pF, $R_S = R_L = 50\Omega$, Figu	re 4 (Note 3)			400	ps
Output Skew Between Ports	tskew	Skew between any two ports: R Figure 4 (Note 3)	, G, B;			350	ps
3dB Bandwidth	f _{MAX}	$R_S = R_L = 50\Omega$, Figure 6			500		MHz
Off-Isolation		$R_S = R_L = 50\Omega$, $V_{IN}_L = 1V_{P-P}$, f Figure 5	= 50MHz,		-58		dB
Insertion Loss	l. oo	1MHz < f < 50MHz,	$\overline{QP} = GND$		0.5		dB
Insertion Loss	ILOS	$R_S = R_L = 50\Omega$	$\overline{QP} = V +$		0.5		αь
Crosstalk	V _{CT}	$f < 50MHz$, $V_{IN} = 1V_{P-P}$, $R_S = R$ Figure 5	$L = 50\Omega$,		-40		dB
Off-Capacitance	Coff	$f = 1MHz, (R,G,B)_0 \text{ to } (R,G,B)_{1,}$	2		6		pF
On-Capacitance	Con	f = 1MHz			10		рF

ELECTRICAL CHARACTERISTICS—3.3V SUPPLY

 $(V+=+3.3V, \overline{QP}=GND, T_A=T_{MIN} \text{ to } T_{MAX}.$ Typical values are at $T_A=+25^{\circ}C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Voltage Range			3.0		3.6	V
Quiescent Supply Current	I ₊	V+ = +3.6V		0.5	1	mA
RGB SWITCHES						
On-Resistance	Ron	$V = +3V$, $V_{IN} = +1.5V$, $I_{IN} = -25mA$		6	7	Ω
On-Resistance Matching	ΔR_{ON}	0 < V _{IN} < +2V, I _{IN} = -25mA (Note 3)		0.8	1.2	Ω
On-Resistance Flatness	R _{FLAT} (ON)	$0 < V_{IN} < +2V$, $I_{IN} = -25mA$		0.9	1.4	Ω
On-Leakage Current	I _L (ON)	R_, G_, B_ = 0V or +3.6V, EN = GND	-1		+1	μΑ
Off-Leakage Current	I _L (OFF)	R_, G_, B_ = 0V or +3.6V, EN = V+		200		рА
LOGIC INPUTS (SEL, \overline{EN} , \overline{QP})						
Input Low Voltage	V.,	V+ = 3.0V			0.8	V
Input Low Voltage	VIL	V+ = 3.6V			0.8	V
Input Lligh Voltage	\/	V+ = 3.0V	2.0			V
Input High Voltage	VIH	V+ = 3.6V	2.0			V
Input Leakage Current	ILEAK		-1		+1	μΑ
ESD PROTECTION						
ESD Protection		Human Body Model, R_, G_, B_		±8		kV
ESD FIOLECTION		Human Body Model, SEL, EN, QP		±2		r.v

AC ELECTRICAL CHARACTERISTICS—3.3V SUPPLY

 $(V+=+3.3V, \overline{QP}=GND, T_A=T_{MIN} \text{ to } T_{MAX}.$ Typical values are at $T_A=+25^{\circ}C$, unless otherwise noted.) (Note 2)

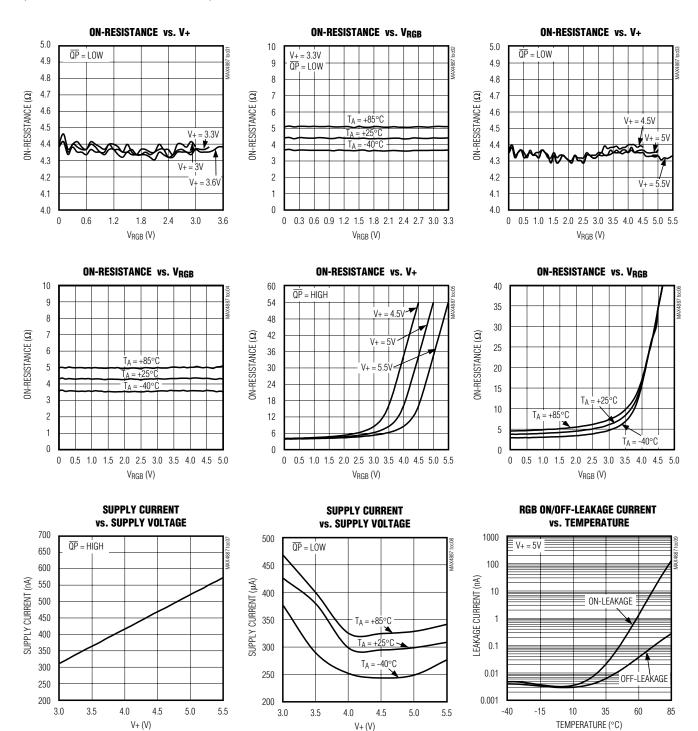
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge-Pump Noise	VQP	$R_S = R_L = 50\Omega$		100		μV _{P-P}
Turn-On Time	ton	V_{IN} = +3V, R_L = 100 Ω , Figure 2			25	μs
Charge Injection		$V_{GEN} = 0V$, $R_{GEN} = 0\Omega$, $C_L = 1.0nF$, Figure 3		21		рС
Propagation Delay	tphl/tplh	$C_L = 10$ pF, $R_S = R_L = 50\Omega$, Figure 4 (Note 3)			400	ps
Output Skew Between Ports	tskew	Skew between any two ports: R, G, B, Figure 5 (Note 3)			350	ps
3dB Bandwidth	f _{MAX}	$R_S = R_L = 50\Omega$, Figure 5		500		MHz
Insertion Loss	ILOS	$1MHz < f < 50MHz, R_S = R_L = 50\Omega$		0.6		dB
Crosstalk	VCT	$f < 50MHz$, $R_S = R_L = 50\Omega$, Figure 5		-40		dB
Off-Isolation		$R_S = R_L = 50\Omega$, V_{IN} = 1 V_{P-P} , $f = 50MHz$, Figure 5		-55		dB
Off-Capacitance	Coff	$f = 1MHz$, $(R,G,B)_0$ to $(R,G,B)_{1,2}$		6		рF
On-Capacitance	Con	f = 1MHz		10	•	рF

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Device is production tested at $T_A = +85^{\circ}C$.

Note 3: Guaranteed by design.

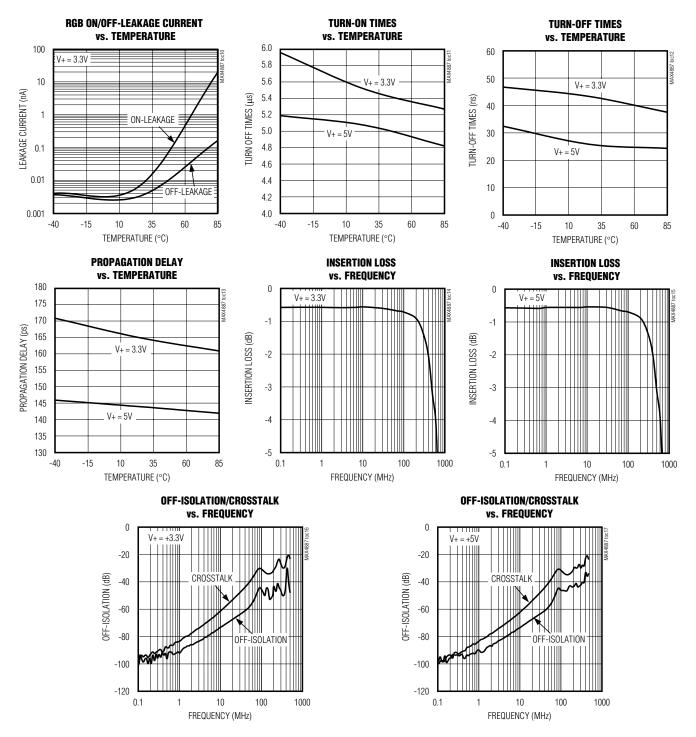
Typical Operating Characteristics

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$



Typical Operating Characteristics (continued)

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$



Pin Description

PIN	NAME	FUNCTION
1	V+	Supply Voltage Input. Bypass V+ to GND with a 0.1µF or larger ceramic capacitor.
2	R0	RGB Input/Output
3	G0	RGB Input/Output
4	В0	RGB Input/Output
5	GND	Ground
6	ĒN	Active-Low Enable Input. Drive EN high to disable the MAX4887. All I/Os are high impedance when the device is disabled. Drive EN low for normal operation.
7, 14	N.C.	Not Internally Connected
8	R1	RGB Input/Output
9	G1	RGB Input/Output
10	B1	RGB Input/Output
11	B2	RGB Input/Output
12	G2	RGB Input/Output
13	R2	RGB Input/Output
15	SEL	Select Input. Logic input for switching RGB switches (see Table 1).
16	QP	Active-Low Charge-Pump Enable. Drive \overline{QP} high to disable the internal charge pump (for V+ = 5V only). RGB switch operates with reduced performance when the charge pump is disabled. Drive \overline{QP} low for normal operation.
EP	EP	Exposed Pad. Connect exposed pad to ground plane.

Detailed Description

The MAX4887 triple, high-frequency switch is intended for notebooks and monitors permitting RGB (red, green, blue) signals to be switched from one driver to one of two loads (1:2) or one of two sources to be connected to one load (2:1). The MAX4887 provides three SPDT high-bandwidth switches to route standard VGA R, G, and B signals (see Table 1).

A boosted gate-drive voltage is generated by an internal charge pump to enhance the performance of the RGB switches. The MAX4887 high-performance switch utilizes n-channel architecture with internal high-drive pullup from a low-noise charge pump resulting in very low on-capacitance. The RGB switches function with reduced performance when the charge pump is disabled (V+ > 5V). The MAX4887's global input $(\overline{\rm EN})$ places all inputs/outputs in a high-impedance state, providing rejection of all signals.

The R_, G_, and B_ analog switches are identical, and any of the three switches can be used to route red, green, or blue video signals. All RGB inputs/outputs are ESD protected to ±8kV Human Body Model (HBM).

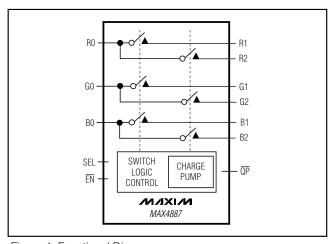


Figure 1. Functional Diagram

Analog Signal Levels

Analog signal inputs over the full voltage range (0 to V+) are passed through the switch with minimal change in on-resistance (\overline{QP} = low). When \overline{QP} = high, the switches can operate within 1V of V+. The switches are bidirectional; therefore, R_, G_, and B_ can be either inputs or outputs.

Timing Diagrams/Test Circuits

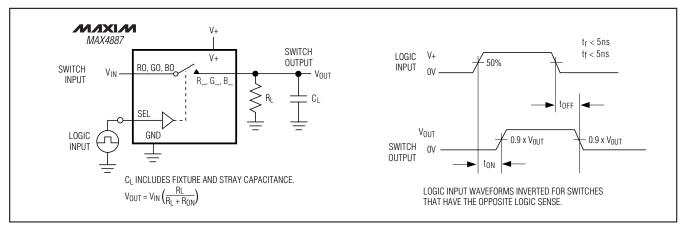


Figure 2. Switching Time

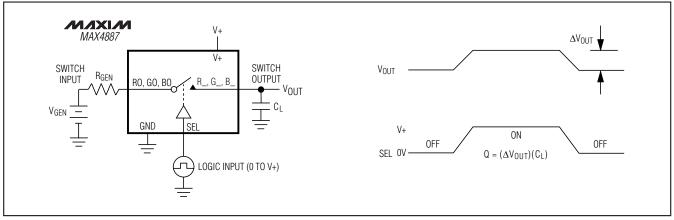


Figure 3. Charge Injection

Charge Pump

A low-noise charge pump with internal capacitors provides a doubled voltage for driving the RGB analog switches when operating the MAX4887 at low voltages (V+ < 5V). The charge pump adds less than 163 μ VP-P of noise to the switches. When operating with V+ = 5V, the charge pump can be disabled to further reduce noise; however, the analog switch's performance is slightly degraded resulting in higher RON and insertion loss. Drive $\overline{\text{QP}}$ high to disable the charge pump. Drive $\overline{\text{QP}}$ low for normal operation.

When operating the MAX4887 at 3.3V, connect $\overline{\text{QP}}$ to GND.

Logic Inputs (EN, SEL)

The MAX4887 has two logic inputs that control the switch configuration and on/off function. Use SEL to switch (RGB)₀ to (RGB)₁ or (RGB)₂. Use $\overline{\text{EN}}$ to connect the switch inputs to the outputs. Drive $\overline{\text{EN}}$ low to enable the RGB switches inputs/outputs. Drive $\overline{\text{EN}}$ high to place all inputs/outputs in a high-impedance state. Table 1 illustrates the MAX4887 truth table.

Table 1. Switch Truth Table

ĒN	SEL	FUNCTION
0	0	(RGB) ₀ to (RGB) ₁
0	1	(RGB) ₀ to (RGB) ₂
1	X	R_, B_, and G_ High Impedance

Timing Diagrams/Test Circuits (continued)

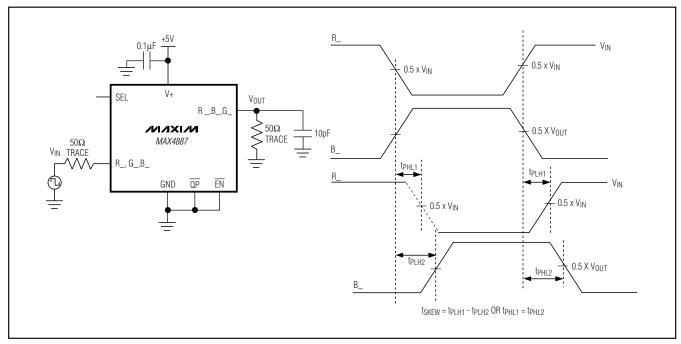


Figure 4. Propagation Delay and Skew Measurement

Applications Information

Power-Supply Bypassing and Sequencing

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence V+ on first, followed by R_, G_, or B_ and the logic inputs. Bypass V+ to ground with a 0.1µF or larger ceramic capacitor as close to the device as possible.

Lavout

High-speed switches such as the MAX4887 require proper PC board layout for optimum performance. Ensure that impedance-controlled PC board traces for high-speed signals are matched in length and as short as possible. Connect the exposed paddle to a solid ground plane.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated to protect against electrostatic discharges encountered during handling and assembly on all pins. Additionally, the MAX4887 is protected to $\pm 8kV$ Human Body Model (HBM) on all switches.

Human Body Model

Several ESD testing standards exist for measuring the robustness of ESD structures. The ESD protection of the MAX4887 is characterized with the Human Body Model. Figure 6 shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage, then discharged through a 1.5k Ω resistor. Figure 7 shows the current waveform when the storage capacitor is discharged into a low impedance.

ESD Test Conditions

ESD performance depends on a variety of conditions. Please contact Maxim for a reliability report documenting test setup, methodology, and results.

Additional Applications Information

Figure 8 illustrates the MAX4887 being used in a laptop in a 2:1 configuration (one of two sources connected to a load). The switch assumes the dedicated DVD player chip outputs R, G, B video, and the MAX4887 switches between normal VGA graphics and the dedicated DVD device.

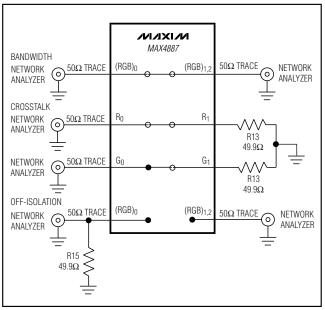


Figure 5. On-Loss, Off-Isolation, and Crosstalk

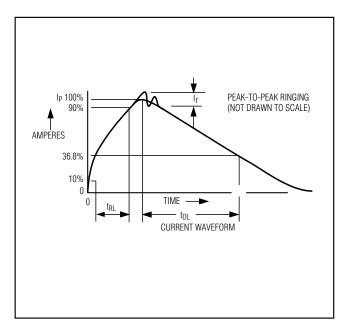


Figure 7. HBM Discharge Current Waveform

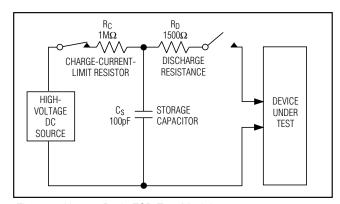


Figure 6. Human Body ESD Test Model

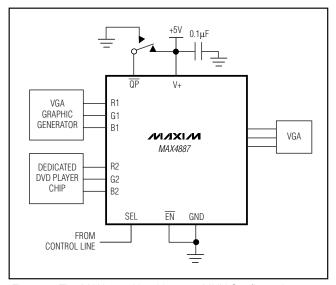
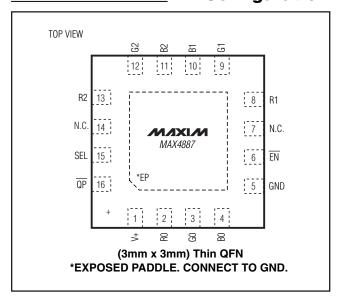


Figure 8. The MAX4887 Used in a 2:1 MUX Configuration

Pin Configuration

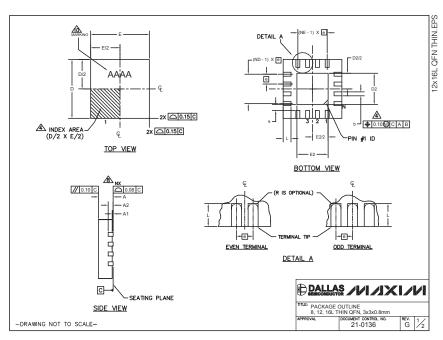
_Chip Information

PROCESS: BICMOS



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



PKG	_	8L 3x3			2L 3x3			L 3x3				EXF	POSE	D PAI) VAF	RIATIC	NS		
REF.	-	NOM.			NOM.	\Rightarrow	MIN.	\rightarrow		PKG.		D2			E2				DOWN
Α	0.70	_	0.80	0.70	-	0.80	_	_	.80	CODES	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	PIN ID	JEDEC	BONDS ALLOWED
b	0.25	0.30	0.35	0.20	_	0.30	_	_	.30	TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC	NO
D	2.90	3.00	3.10	2.90		3.10	_	_	.10	T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
E e	2.90	3.00 .65 BS	3.10	2.90	3.00 50 BSC	3.10		3.00 50 BSC	.10	T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
L	-	0.55	_	_		0.65	0.30		50	T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
N	0.33	8	0.75	0.45	12	0.05	0.30	16	.50	T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
ND	+	2			3	\rightarrow		4	_	T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
NF	+	2			3			4	\dashv	T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
A1	0	0.02	0.05	0		0.05	0	0.02	05	T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
A2	+-	.20 RE		_	20 RFF	-		20 RF	.00	T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
k	0.25	-		0.25	- 1		0.25	- 1	_										
										4.5M-1994.									
	1. DIM 2. ALI 3. N II 4. TH JES WI MA 6. DIM FR 6. ND 7. DE 6. CO	L DIME S THE E TER SD 95- THIN T RKED MENSIO OM TE AND I POPULIPLAN	NSION TOTAL MINAL 1 SPP- HE ZO FEATI ON b A RMINA NE REI LATION ARITY	NS ARI L NUM #1 IDE 012. [DNE IN URE. PPLIE AL TIP. FER TO APPLII	E IN MI BER O ENTIFIE DETAIL DICATE S TO M	LLIME F TER ER AN S OF " ED. TH METAL NUMB E IN A THE E	TERS. MINAL: D TERI TERMINIE TER LIZED ER OF A SYMM XYPOSE	ANGL S. MINAL MINAL TERM TERM TERM ED HE	S ARE IN I NUMBERIN IDENTIFIE #1 IDENTII IAL AND IS NALS ON I AL FASHIO T SINK SL	DEGREES. IG CONVENTION R ARE OPTIONA FIER MAY BE EI S MEASURED BE EACH D AND E S	L, BUT THER A ETWEEN	MUST I MOLD N 0.20 n SPECT	BE LOC OR nm ANE	ATED	ım				

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